Fairchild Imaging CIS 2521F

Standard and Scientific Package Datasheet

5.5 Megapixel CMOS Image Sensor

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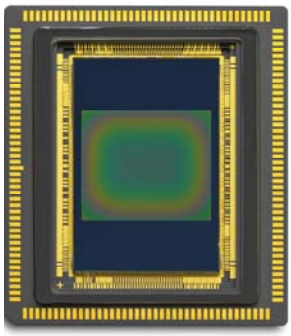
PRODUCT DESCRIPTION （Rev： E）

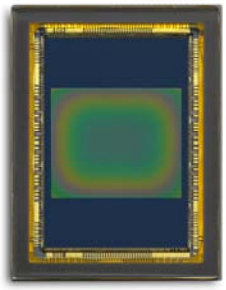
The Fairchild Imaging CIS2521F is a large format, ultra low-noise CMOS image sensor intended for scientific and industrial applications requiring high quality imaging under extremely low light conditions. The device features an array of 5 transistor (5T) pixels on a 6.5µm pitch with an active imaging area of 2560(H) x 2160(V) pixels. The sensor runs in Rolling Shutter and Global Shutter readout modes. The sensor has two ADC channels per column with one optimized for very low light levels and the other optimized for high light levels, allowing high dynamic range data collection in a single image. The sensor supports user-programmable row start/stop control for region of interest (ROI) readout mode. The CIS2521F delivers extreme low-light sensitivity with a read noise less than 2 electrons RMS, Quantum Efficiency (QE) above 55%, and very low dark current. These features, combined with 5.5 megapixel resolution and 100 fps imaging rates, make the CIS2521F an imaging device ideally suited for a variety of high throughput, low light-level imaging applications.

CIS2521F0121



Scientific 168 pin CLCC

CIS2521F0221



Standard 168 pin CLCC

The CIS2521F sensor is available in a 168 pin Scientific package (CIS2521Fx121), or in a 168 pin Standard package (CIS2521Fx221). For this datasheet, both packaged options are specified. The Scientific package is shown above on the left and the Standard package is shown above on the right.

FEATURES	BENEFITS
2560 (H) x 2160 (V) pixel CMOS Image Sensor	5.5 Megapixels of data
6.5 µm x 6.5 µm pixel area	Ideal pixel size for maximum light collection
Maximum frame rates: -100 fps in Rolling Shutter readout mode - 50 fps in Global Shutter readout mode	Precise capture of dynamic events
< 2 e- RMS Readout Noise	Enables ultra low-light imaging
Programmable ROI readout	Flexible windowing to allow faster frame rates
< 35 e-/pixel/sec dark current @ 20°C	Cooling not required for dynamic applications
≥ 55% peak Quantum Efficiency (QE)	High sensitivity from visible through NIR
> 83.5 dB intra-scene dynamic range	Record intense & faint features simultaneously
On-chip column parallel 11-bit A/D converters Dual gain 11-bit output channels per pixel	Digital sensor for more compact designs

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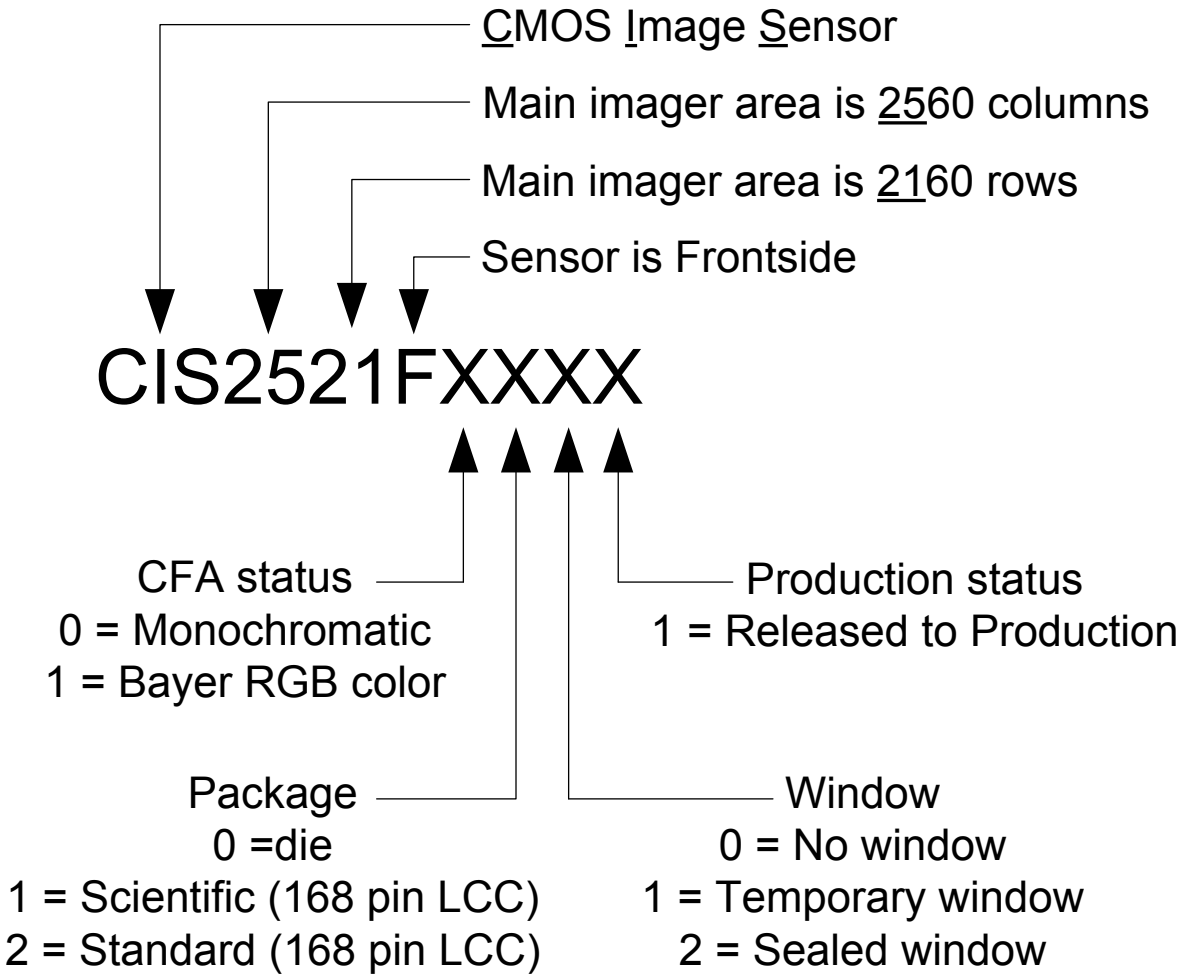
Sensor naming convention



This datasheet will describe the monochromatic and color options for the Scientific and Standard packages. Drawings will assume that the Sealed window option is always used. So, effectively this datasheet covers the four parts CIS2521F0121, CIS2521F1121, CIS2521F0221, and CIS2521F1221.

At the time of this datasheet revision (February 2013), the Backside CIS2521 is not in production. Therefore this datasheet will sometimes use “CIS2521” and “CIS2521F” interchangeably.

General Specifications

Parameter	Typical value
Active array size	2560 (H) x 2160 (V), imaging pixels only 2592 (H) x 2192 (V), imaging and dark pixels
Pixel size	6.5 µm x 6.5 µm
Dimensions of active area (Note 1)	16639.6 µm (H) x 14039.6 µm (V), imaging pixels only 16847.6 µm (H) x 14247.6 µm (V), imaging and dark pixels
Dimensions of die (Note 2)	18842 µm (H) x 27642 µm (V), die circuit only 18882 µm (H) x 27682 µm (V), including seal ring 19002 µm (H) x 28122 µm (V), including saw street (estimate)
Shutter type	Rolling Shutter, Global Shutter (snapshot). ROI readout capabilities for both shutter types.
Maximum frame rate (Note 3)	100 fps (Rolling Shutter) 50 fps (Global Shutter)
Number of readout ports	2 (1 for top half array, 1 for bottom half array)
Maximum line rate (Note 3)	109.6 kHz (9.124 µs/line)
Maximum pixel rate (Note 3)	284 MHz (3.48 ns/pixel)
ADC resolution	2 x 11-bit
Column level amplifier gain	1x or 2x (low gain output) 10x or 30x (high gain output)
Power consumption	< 2 W
I/O interface	1.8V LVCMOS and 1.8V HSTL (class I)
Package type	168-pin LCC

Note 1: Dimensions are from the lithographic pattern.

Note 2: The dimensions for the die circuit area and the seal ring around it are defined by lithography and are accurate to sub-micron tolerances. When the die is cut from the wafer, there may be greater variations depending on the wafer cut process.

Note 3: The values for line rate and pixel rate are calculated values based on the assumption of 100 fps operation. If the sensor is running 100 fps, one frame takes 0.01 seconds and there are 1096 lines in a frame (for each sensor half, assuming the default frame size). Therefore each sensor half has a maximum line rate of 109.6 kHz. Each line has 2592 pixels, so the maximum pixel rate is (2592 pixels/line)*(1096 lines/frame)*(100 frames/sec) = 284,083,200 pixels/second, or 284 MHz.

Because these values for maximum pixel and line rates are calculated values, what the actually showing is maximum average line rate and maximum average pixel rate. On chip, the maximum SCLK input is 287 MHz, and the digital numbers for each pixel value come out one per SCLK (for each imager half). So actual pixel data may be appearing on the DOUT and DOUT_LG pins at

the SCLK rate of 287 MHz, at least for the portion of each line time that pixel readout is occurring (2592 SCLKs out of every 2624 SCLKs).

If the 100 fps number is not assumed but is instead calculated from on-chip functionality, a slightly different fps number can be found. In the CIS2521 sensor, the number of clocks per row of pixels is set by JTAG Registers 16 through 47, which together are called the “wavetable”. According to both default and recommended wavetable settings, there are 2624 clocks per line. This then correlates to a line time of (2624 clocks/line)/(287 million clocks/sec) = 9.142 µs/line. The maximum frame rate then depends on the number of lines in the frame. The number of lines in the frame are controlled by the user loading values into JTAG Registers 6, 7, and 8. With the default values that are automatically loaded at device start up, the frame is 1080 imager lines plus 16 dark lines = 1096 lines. So the Rolling Shutter maximum frame rate with default settings is:

(287 million clocks/sec) / (2624 clocks/line)*(1096 lines/frame) = 99.79 frames/second

which we round up to 100 fps in the above table. (Obviously much higher frame rates are possible if smaller frame sizes are used in place of the default 1096 lines.) Note that the actual image with the default settings will actually be 1096*2 = 2192 rows high, since the “1080” and “16” numbers are with respect to the imager half, and the final image consists of both halves.

The maximum frame rate for Global Shutter is always ½ the number for Rolling Shutter, since two frames of sensor readout (the Reset and Data frame) are necessary to construct the final Global Shutter image.

Electrical-optical specifications

Parameter	Specification	Notes
Intra-frame dynamic range	15000:1	
PRNU	< 3% RMS	at 75% of max output
Dark current	< 35 e-/pixel/sec	at 20ºC
Dark current non-uniformity	< 65 e-/pixel/sec RMS	at 20ºC
Fixed pattern noise (FPN)	< 2% RMS	of the max output
Conversion gain (DN/e-)	High gain output (nominal): − 1.7 at 30x − 0.57 at 10x Low gain output (nominal): − 0.12 at 2x − 0.06 at 1x	ADC input range is programmable from 0.4V to 1.55V. So, conversion gain in DN/e- is programmable.
Full well capacity (FWC)	≥ 30,000 e-	
Lag	< 0.1%	of maximum output
Non-linearity	< 2%	
Fill factor with microlens	> 0.9	
Microlens F#	1.5 for monochromatic sensor 1.6 for color sensor	
Peak QE	≥ 0.55	at 600nm
MTF	≥ 0.4	at 600nm
Temporal read noise	< 2 e- RMS @ 30 fps Rolling Shutter readout	Median value of read noise distribution from high gain output (30x gain)
Spectral sensitivity range	400 – 700nm	See QE plots (Figure 29 and Figure 31) for spectral sensitivity in the Near IR out to 1100 nm

The above specifications are from CIS2521F devices running in Rolling Shutter mode. Although the CIS2521F runs in Global Shutter mode, BAE does not guarantee any performance specifications for Global Shutter mode. However, the functionality of all sensors to operate in Global Shutter mode is verified at wafer test.

For sensor performance specifications in photometric units, contact Technical Support at cams.techsupport@baesystems.com.

Recommended Operating Conditions

Parameter	Definition	Min	Nom	Max	Units
AVDD	Analog circuits power supply (avg 250 mA, Peak at 355 mA on 5% duty cycle) Note 1	3.135	3.3	3.465	V
AVDD_PIX	Pixel source follower power supply (25 mA nom)	3.135	3.3	3.465	V
AVDD_RST1	Pixel reset power supply1 (1 mA)	2.2	3.00	3.3	V
AVDD_RST2	Pixel reset power supply2 (1 mA)	2.2	3.00 (RS) or 2.739 (GS) (Note 2)	3.3	V
DVDD_3V3	Row circuits and level shifters power supply (1mA)	3.135	3.3	3.465	V
DVDD	Digital circuits power supply (290 mA @287MHz)	1.71	1.8	1.89	V
DVDD_IO	I/O circuits power supply (270 mA @287MHz) Note 3.	1.71	1.8	1.89	V
VTX1_POS	TX1 Transfer gate positive power supply (1mA in Rolling Shutter, 200 mA for 1µsec/pulse during Global Shutter)	2.90	3.3	3.60	V
VTX2_POS	TX2 Transfer gate positive power supply (1mA in Rolling Shutter, 200 mA for 1µsec/pulse during Global Shutter) (Note 4)	2.90	3.3	3.60	V
VTX1_NEG	TX1 Transfer gate negative power supply (same current max as VTX1_POS)	-1.5	-0.4	+0.3	V
VTX2_NEG	TX2 Transfer gate negative power supply (same current max as VTX2_POS)	-1.5	-0.4 or +0.8 (Note 5)	+0.85	V
$T_{operation}$	Sensor junction temperature	-40	30	+55	°C
RTRIM	Bias resistor for bandgap based internal bias generator (current through resistor is approximately 100µA; for low noise, place resistor close to sensor)	11K	12.28K (Note 6)	13.5K	Ω
PTAT R_{OUT}	Output resistance of PTAT temperature sensor		100K (Note 7)		Ω

Note 1: The relevant period for this duty cycle is the row readout time, which is 2624 SCLKs for both the default and recommended wavetables. The 5% number comes from the percentage of clock cycles that buff_en (wavetable bit 8) is high during the 2624 SCLK row readout time.

Note 2: The recommended voltage for AVDD_RST2 is 3.00 Volts when running in Rolling Shutter and 2.739 Volts when running in Global Shutter. If the user plans on switching between Rolling and Global Shutter, the power to AVDD_RST1 must be switchable between these two

voltages. For Global Shutter operation, it is critical for there to be a tightly controlled differential between AVDD_RST1 and AVDD_RST2 – a 261 mV differential in the case of AVDD_RST1 = 3.000 V and AVDD_RST2 = 2.739 V. This is particularly critical for high gain Global Shutter operations. This differential voltage controls the DN level of the Reset frame, with a target of about 300 DN for the Reset frame being the goal. At 10x gain, each 10 mV of differential voltage changes the Reset level by 100 DN. At 30x gain, each 10 mV of differential voltage changes the Reset level by 300 DN.

Note 3: Normally the DOUT and DOUT_LG pins send their outputs to another chip (typically an FPGA) to be decoded from Gray code to binary. If the traces connecting the imager to this external chip are too long, the user may wish to add termination at the inputs to this other chip to prevent signal reflection. Adding such termination will increase the current requirement on DVDD_IO. (In practice, no BAE-designed cameras have required such termination.)

Note 4: In Rolling Shutter, the TX2 gate is not typically pulsed and the TX1 gate only gets pulsed for one row of pixels at a time. The current requirements of VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG are therefore minimal (< 1 mA) in typical Rolling Shutter applications. In Global Shutter, both the TX1 and TX2 gates pulse globally (i.e. every pixel in the sensor pulsing simultaneously). In Global Shutter therefore, VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG all must have enough current capacity to source or sink the necessary currents. For a Global TX2 pulse, the VTX2_POS must supply 200 mA on the rising edge of that pulse and the VTX2_NEG must sink 200 mA on the falling edge of that pulse. Similarly, for a Global TX1 pulse, the VTX1_POS must supply 200 mA on the rising edge of that pulse and the VTX1_NEG must sink 200 mA on the falling edge of that pulse. At a minimum, Global Shutter operation typically requires a single Global TX2 pulse and a single Global TX1 pulse. But sometimes (see Figures 17 and 22) there are Global TX2 pulse trains where these 200 mA source/sink current requirements are needed each line time. The 200 mA number is for the imager as a whole. The number for each imager half is 100 mA.

Note 5: The recommended voltage for VTX2_NEG is -0.4 Volts when running in Global Shutter. -0.4 Volts is also recommended when running in Rolling Shutter under low light conditions. But when running in Rolling Shutter under high light conditions, +0.8 Volts is recommended. This voltage setting will make use of the TX2 gate's anti-blooming functionality

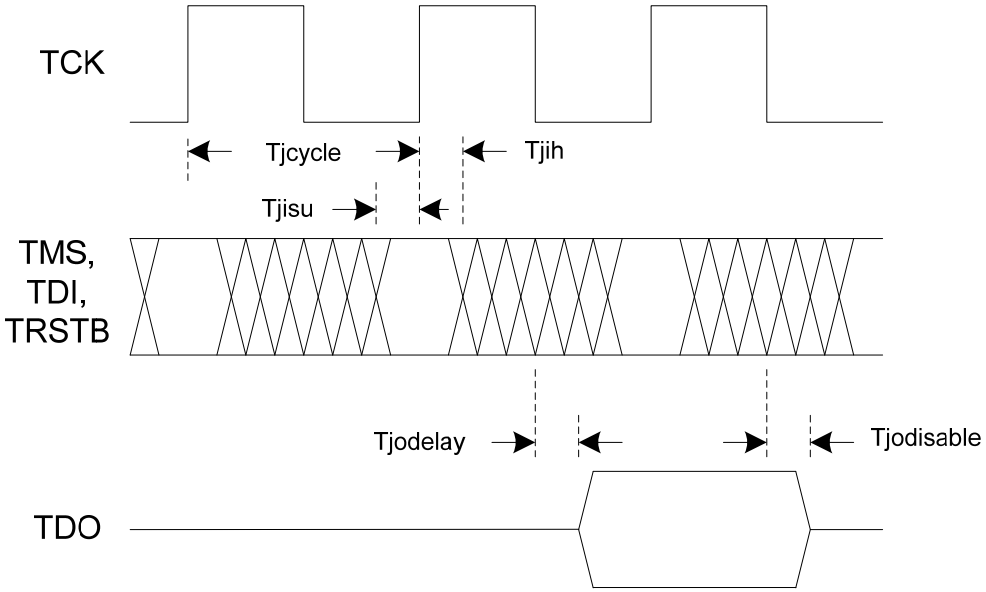
Note 6: There are two RTRIM pins on the packaged part, pins 75 and 96. For each pin, a 12.28 KΩ resistor should be attached with one end to the RTRIM pin and with the other end at analog ground. These two resistors are important in order to power the column amplifier circuits and insure functioning DOUT and DOUT_LG outputs.

Note 7: The 100KΩ resistance is an internal resistance inside the chip. The user does not need to add any external resistor. The 100KΩ number is given so that when the user measures the PTAT voltage, the user will choose a voltmeter with an internal impedance much greater than 100KΩ so as not to load the PTAT pin and get an inaccurate voltage reading. PTAT stands for Proportional To Absolute Temperature.

Timing Specifications

JTAG Interface

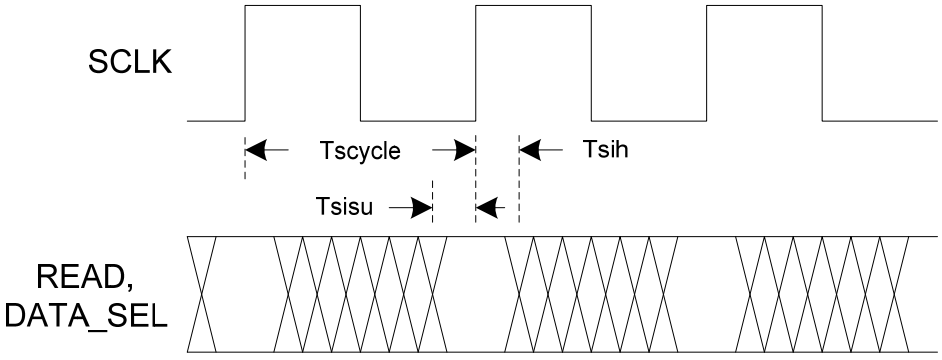
Figure 1. JTAG Interface I/O Timing



Parameter	Definition	Unit	Min	Max	Note
Tjcycle	TCK clock cycle time	ns.	40		
Tjdc	TCK clock duty cycle	%	45	55	
Tjisu	JTAG input setup time for TMS, TDI, and TRSTB	ns.	2.0		
Tjih	JTAG input hold time for TMS, TDI, and TRSTB	ns.	1.0		
Tjodelay	JTAG output delay time for TDO signal from falling edge of TCK	ns.		8.0	
Tjodisable	JTAG output disable time for TDI signal from falling edge of TCK	ns		6.0	

Functional Control Inputs

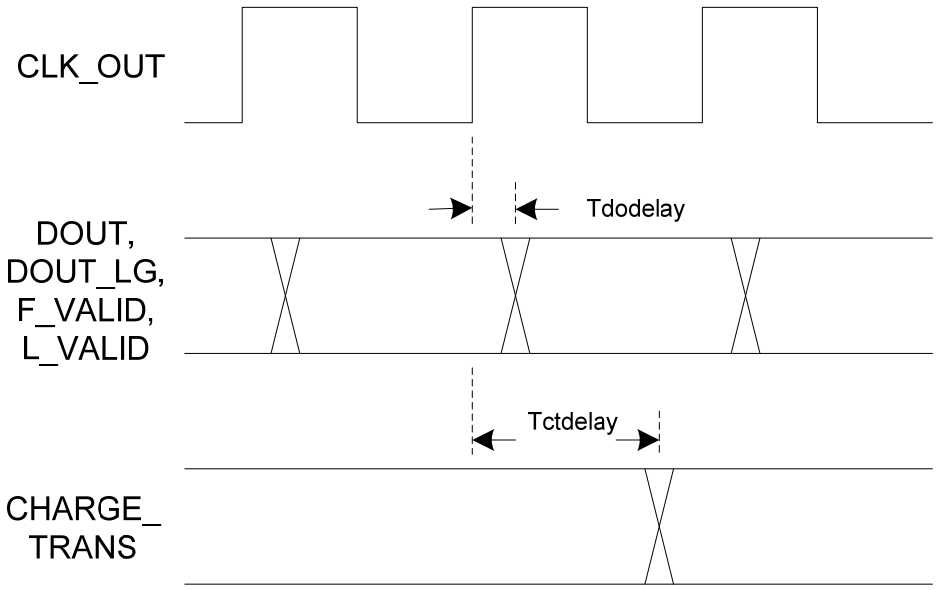
Figure 2. Functional Control Inputs Timing



Parameter	Definition	Unit	Min	Max	Note
Tscycle	SCLK clock cycle time	ns.	3.48		
Tsdc	SCLK clock duty cycle	%	48	52	
Tsjitter	SCLK peak to peak cycle jitter	ps.		150	
Tsisu	READ, DATA_SEL input setup time	ns.		1.0	
Tsih	READ, DATA_SEL input hold time	ns.		0.5	

Data and Status Outputs

Figure 3. Data and Status Output Timing

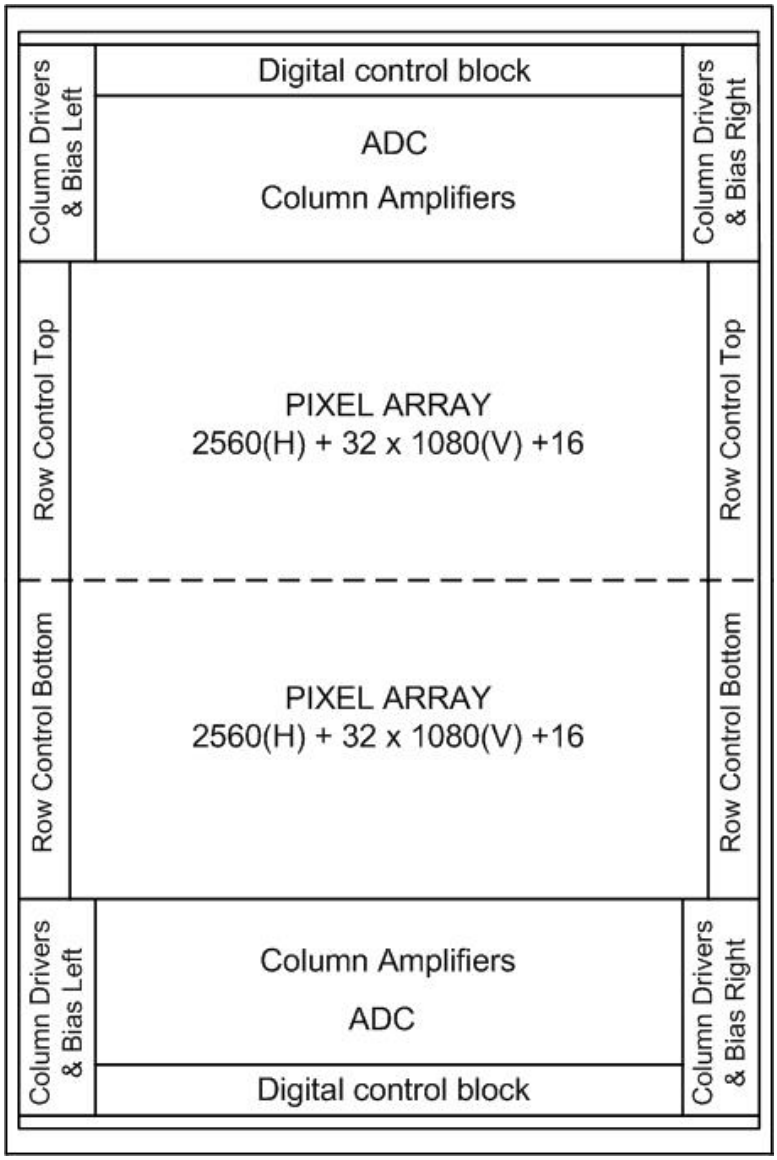


Parameter	Definition	Unit	Min	Max	Note
Tdodelay	DOUT, DOUT_LG, F_VALID, L_VALID output delay time	ns		1.0	Source Synchronous
Tctdelay	CHARGE_TRANS output delay time	ns		2.5	

Device Architecture

Sensor Floor plan

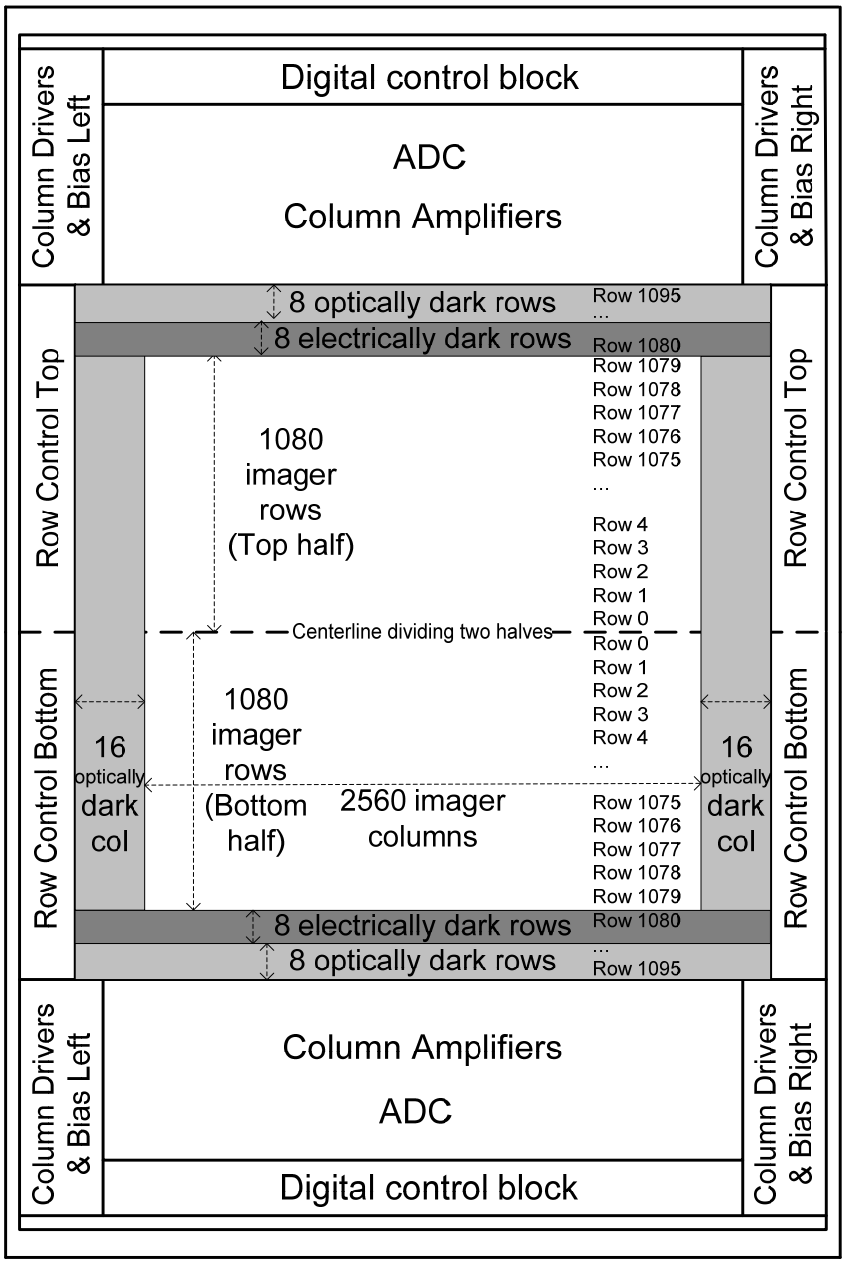
Figure 4. Floor Plan of the CIS2521 Image Sensor



The CIS2521 floor plan is shown in Figure 4. The sensor consists of two independent halves. The pixel orientation is identical in both halves. The column amplifier circuits, ADCs and the digital control block (DCB) are located at the top and bottom of the array. The row control circuits are located on both sides of the pixel array.

The 2560 by 2160 active imager pixel array is surrounded on all sides by a 16 pixel wide dark region. Rows are numbered with row 0 in the center and with numbers increasing moving outward from the center. Because the two imager halves are to be treated independently, the top and bottom halves use the same row numbering scheme without contradiction.

Figure 5. CIS2521 sensor floor plan with row numbering



The optically dark rows are covered with metal so light cannot enter. The electrically dark rows are also covered with metal so light cannot enter; but in addition, all the pixels of these rows have the gates of their TX2 transistors permanently tied to AVDD. This makes them “electrically dark” as well as “optically dark”, because any charge in these dark rows (from dark current, for example) is removed via the TX2 charge dump, which is permanently active for these rows.

Sensor Architecture

Figure 6. Architecture of each half of the CIS2521

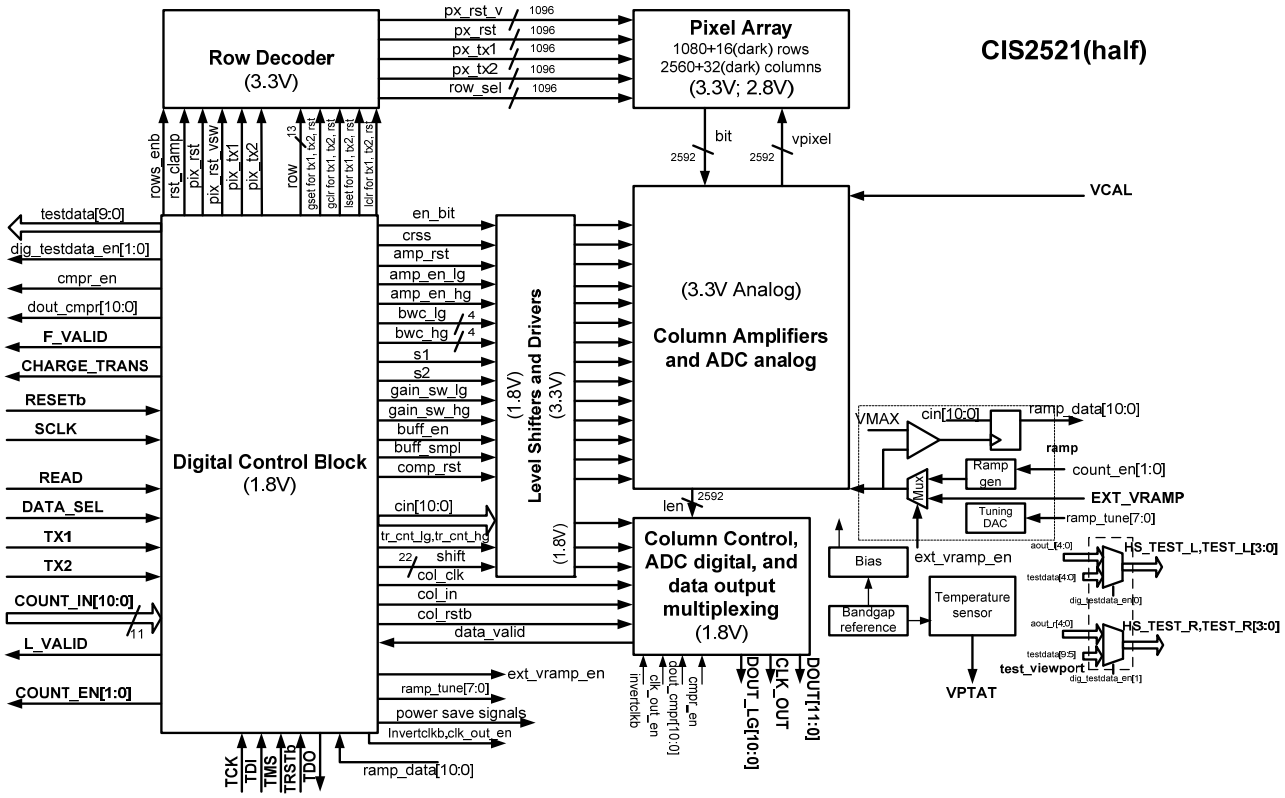


Figure 6 illustrates the architecture of each half of the sensor. The DCB includes all of the digital circuits required for programming and controlling the device. The DCB contains five major sub-sections: the JTAG tap controller, the JTAG registers, the Gray code ramp counter, the row controller, and the waveform generator.

The row decoder consists of a 13-bit decoder and 1096 row-driver circuits that control each row of pixels. There are five output signals for each pixel row: PX_TX1, PX_TX2, PX_RST, PX_RST_V, and ROW_SEL.

Column control signals are generated in the DCB and routed to the “Level Shifters and Drivers” on both sides of the column circuitry. The “Level Shifter and Drivers” convert incoming 1.8V LVCMOS signals into 3.3V LVCMOS signals for controlling the column level amplifiers and ADCs. This block also contains the bias generator circuitry. There are two bias references that can be selected via JTAG Register 9, bit 25. The first bias reference, based on the internal bandgap reference voltage, allows the bias point to be changed via an external resistor RTRIM. It achieves the minimum bias variation as a function of temperature (Register 9, bit 25 = 0, the default). The second bias reference, based on an internal resistor, achieves the lowest readout noise (Register 9, bit 25 = 1). Even if the internal resistor is used by setting Register 9 bit 25 to 1, external RTRIM resistors at pins 75 and 96 should still be added.

Separate power supplies are used for the pixel core, analog amplifiers and ADCs, the pad ring, and the digital circuitry. A voltage ramp generator is integrated on the sensor to drive the single

slope ADCs in each column. The offset and swing of the ramp generator can be programmed via the JTAG interface.

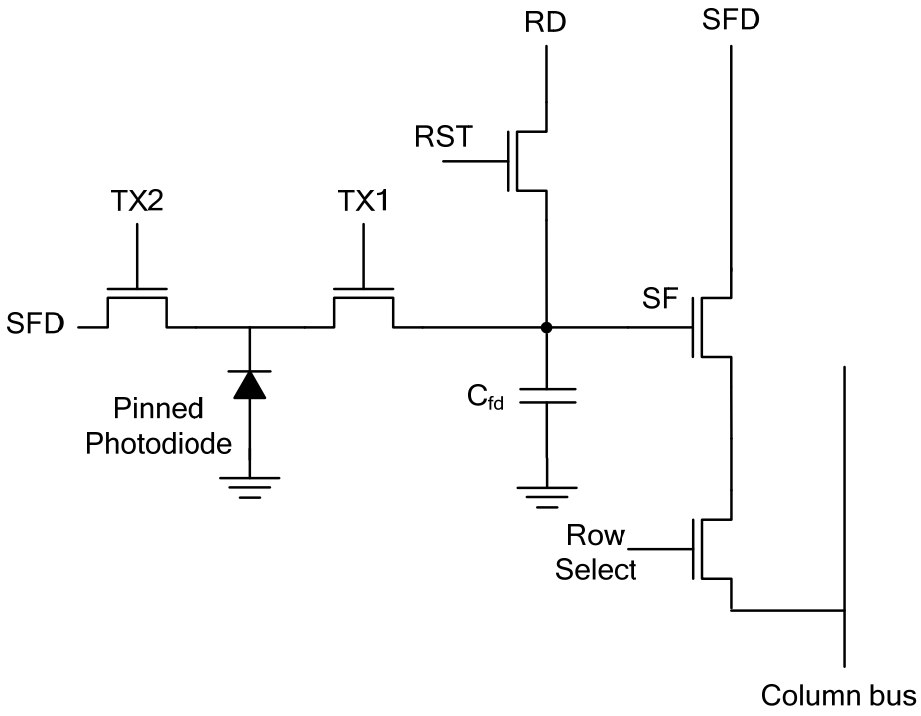
The user must provide a system clock which synchronizes all the operations in the chip. The row and column control clocks, and the built-in Gray code counter for the single slope ADCs are all derived from the system clock.

The user has the ability to change the timing of the internal control signals by reprogramming the JTAG registers.

An on-chip PTAT temperature sensor provides a continuous analog output voltage for monitoring the die temperature.

Pixel architecture

Figure 7. 5T pixel schematic



A schematic diagram of the 5T pinned photodiode pixel is shown in Figure 7. The pinned photodiode inside of each pixel starts to integrate charge as soon as the transfer gate TX1 is turned off. Then when the transfer gate TX1 is turned on, the integrated charge in the photodiode is dumped onto the floating diffusion node and read out as a voltage signal by the source follower. The TX2 gate serves both as a global reset gate and a lateral anti-blooming protection gate.

Column readout circuitry

Figure 8. Column readout circuitry

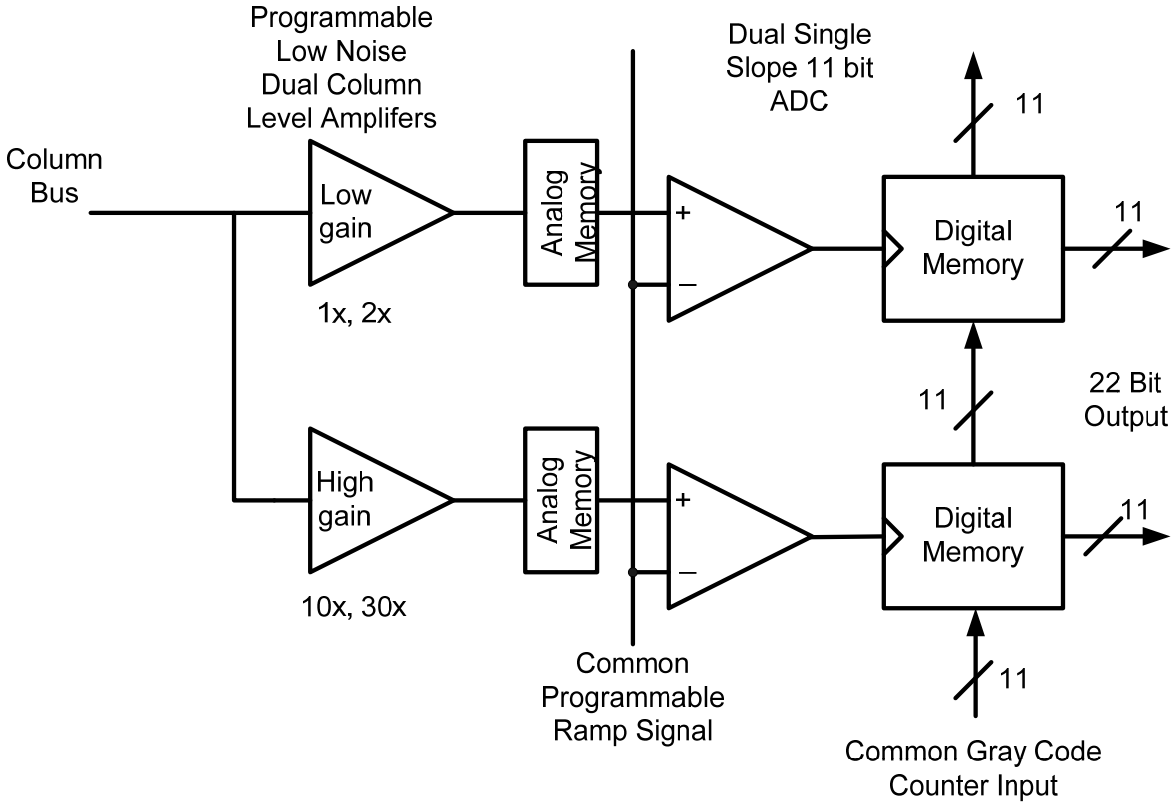


Figure 8 shows the amplifier and ADC structure used in each column of the sensor. This architecture was selected to minimize the sensor read noise while maximizing dynamic range.

There are two amplifiers per column simultaneously generating low gain and high gain output signals. The gain of each amplifier is selected to either maximize the full well capacity, i.e. 1x gain, or to minimize the read noise, i.e. 30x gain. The amplifier output gain is further controlled by the settings of the gain_sw_lg and gain_sw_hg signals (via JTAG Register 2, bits 4 and 5). When gain_sw_lg is set to 1, the low gain output is 1x, if gain_sw_lg is set to 0, then the low gain output is 2x. On the other hand, when gain_sw_hg is set to 1, the high gain output is 10x and when gain_sw_hg is set to 0, the high gain output is 30x.

In addition to gain, the bandwidth of the column level amplifiers is also programmable via JTAG Register 2, bits 6 to 13. Each column also contains two 11-bit single slope ADCs. The outputs of the amplifiers and the outputs of the ADCs are double buffered to maximize the line rate of the sensor.

The data output bus is 22 bits wide with DOUT_LG[10:0] representing the low gain data and DOUT[10:0] representing the high gain data. Because the counter input to the ADC is in Gray code, the DOUT[10:0] and DOUT_LG[10:0] outputs will be in Gray code. The user will have to convert these outputs from Gray code to binary off-chip.

Sensor Data

After the analog pixel data is digitized, the 22-bit pixel Gray code output data is sent out through two registers to the output pads. The low gain data are delivered at the 11-bit output port DOUT_LG[10:0], and simultaneously, the high gain data are presented at the 11-bit output port DOUT[10:0].

A source synchronous output clock CLK_OUT is provided with the output data. CLK_OUT is used to register DOUT_LG[10:0] and DOUT[10:0]. CLK_OUT can be inverted or disabled via a JTAG register.

Sensor Interface

JTAG Interface

Name	Direction	Description
TCK	Input	JTAG clock
TDI	Input	JTAG serial data input
TMS	Input	JTAG mode select control
TRSTB	Input	JTAG state machine reset (active low)
TDO	Output	JTAG serial data output

Control Signals

Name	Direction	Description
DATA_SEL	Input	Selects between a Data (1) or Reset (0) frame readout in Global Shutter mode. Toggling this signal also switches between wavetable A (0) and B (1). JTAG write access to the wavetable is the complement of the table being used for readout. This input is not used for frame selection in Rolling Shutter mode since the distinction between Reset frame and Data frame is not relevant, though it is set to DATA_SEL = 0 in Rolling Shutter because Rolling Shutter uses wavetable A.
READ	Input	READ has multiple functions depending on the sensor's mode of operation. It controls external start/pause of the row counter and readout activities in internally triggered readout modes. It is also used for external triggering in external triggered readout mode. It can also be used to synchronously reset the sensor operation.
RESETB	Input	Active low reset input (asynchronous). RESETB = 0 resets the sensor and loads the JTAG registers with default values.
SCLK	Input	System clock input
CHARGE_ TRANS	Output	Marker pulse indicating when data sampling is occurring for the selected row. This signal comes directly from the wavetable without any modification.
F_VALID	Output	Frame valid output, high from beginning of first row to end of last row including dark rows but not pre-scan rows. The timing of rising and falling edge is from the wavetable.

Name	Direction	Description
L_VALID	Output	Line valid output indicates valid line data. This signal comes directly from the wavetable.

Global Shutter Readout Mode Pixel Control

Name	Direction	Description
TX1	Input	Global Shutter readout mode charge transfer pulse.
TX2	Input	Exposure control / charge dump signal. Although not generally used for Rolling Shutter (see Figures 14, 15, and 20), this signal can have the same exposure control function in Rolling Shutter mode (see Figure 21).

Please refer to the CIS2521 Programming Manual for additional information.

Power up sequence

We recommend that the power up sequence follows the order shown below:

1. First, DVDD and DVDD_IO should be powered-up with all the analog supplies held low, with DVDD_3V3 held low, and with both RESETB and READ held low.
2. Next, SCLK should be activated (SCLK_TP and SCLK_BT if running both halves) for a minimum of 8 cycles before proceeding.
3. Then, the sensor should be taken out of reset with both RESETB and READ going high. If both sensor halves are to be frame-synchronized, the READ_TP and READ_BT signal edges have to be applied simultaneously. SCLK should be clocked for at least one frame time before proceeding to next step.
4. At this point, taking the sensor back into reset is optional. (For example, setting the READ pin to 0 at this point would make it possible to program the registers with non-default values. When this task is done, READ should be set high again.)
5. Now, AVDD and all other analog power supplies can be brought up. DVDD_3V3 is also to be brought up at this time.

Power down sequence

All the power supplies can be brought down simultaneously.

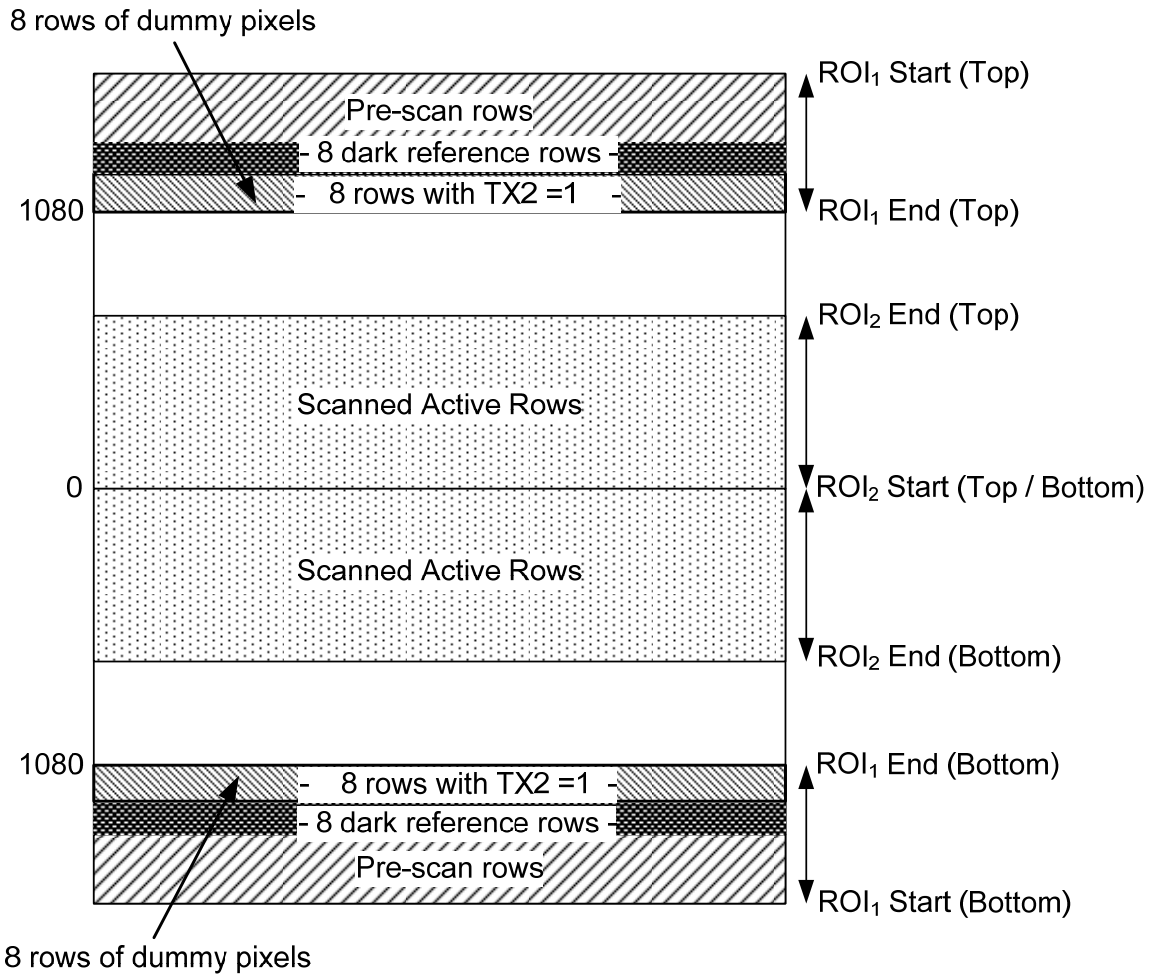
Selective component power down

A JTAG register (address 3) is provided to selectively power down individual circuits in order to reduce noise and power dissipation of the sensor under some modes of operation. This register is activated by setting JTAG Register 2 (mode register) bit 25 (low power activation) to 1.

Readout Modes

Region of Interest

Figure 9. Programmable Regions of Interest



The row control supports two regions of interest (ROI). The first ROI defines the non-imaging region of interest: dark rows and pre-scan rows. It has a programmable size (JTAG Register 8) and a fixed end address of 1080 pointing to the start of the 8 dummy (also called “electrically dark”) rows, the pixels of which are optically shielded and have their TX2 gates tied to AVDD to dump all the charge out. The next 8 rows of the first ROI are dark reference rows where the pixels are covered by an opaque metal light shield. A size of 0 will suppress the output from this first ROI region. The direction of counting is always down, i.e. for a ROI_1 size greater than 0, counting will be from (1079 + size) down to 1080. If the row address is greater than 1095, no actual row is selected and the chip output data would correspond to background noise of the column circuits. This operation is termed “pre-scan”. For the pre-scan rows, the background noise level of the column amplifier circuits is equal to the floating diffusion node voltages of the last row of ROI2 to be read out. (When the number of pre-scan values is large, it is possible for dark current to build up on the floating diffusion nodes over the pre-scan readout period.) Pre-scan rows are also called virtual rows.

The second ROI is the region that contains all the light sensitive pixels. This region is called the active imager region. It has programmable start and end addresses. The counting direction of this ROI is computed automatically from the starting and ending addresses. If the ending address is greater than the starting address, the counting direction is from the center of the imager outward (i.e. up for the top half of the imager, down for the bottom half). Otherwise it is in the reverse direction (i.e. row counting proceeds toward the direction of the imager center). Figure 9 schematically shows the two ROIs in the top and bottom halves of the sensor.

Normally, a frame of data consists of the ROI1 rows preceding the ROI2 rows (pre-scan/dark/active imager). This order can be reversed if Register 2 bit 22 is set to 1 (not the default). In that case, a frame consists of the ROI2 rows followed by the ROI1 rows (active imager/pre-scan/dark).

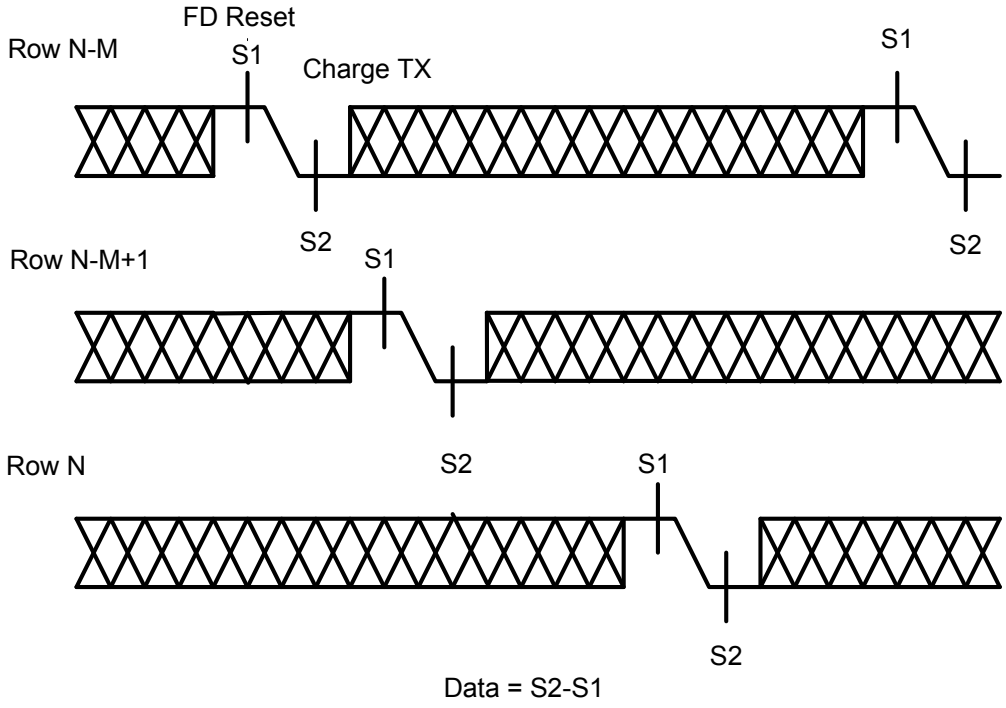
L_VALID is asserted once each row readout, whether that row is pre-scan, dark, or active imager. F_VALID is asserted high once the first physical row of the frame is read out and goes low only after the last physical row of the frame is read out. Physical rows are dark rows and active imager rows. F_VALID will be low and stay low during the readout of pre-scan rows.

Rolling Shutter readout

Rolling Shutter is the standard readout method for CMOS image sensors. When READ is asserted in Rolling Shutter mode, one row at a time is sequentially processed until the frame is completely read out. In video readout mode, i.e. when READ is always asserted, frames are continuously read out, separated only by a programmable frame blanking time. Note that the frame blanking time is determined by the number of pre-scan lines in each image. Readout of each row consists of four separate operations. The first operation is resetting the floating diffusion nodes in each pixel. The second operation is reading the reset voltage out via the source follower transistor in each pixel. The third operation is transferring charge from the pinned photodiode to the floating diffusion node, via TX1, and the last operation is reading out the signal voltage. At the edge of the array, column parallel circuitry amplifies, subtracts, and digitizes the row data. The difference between the reset voltage the signal voltage is a form of correlated double sampling (CDS). CDS removes kTC, i.e. reset, noise on the floating diffusion node, and suppresses the source follower 1/f noise. This readout mode achieves the lowest read noise available for the CIS2521.

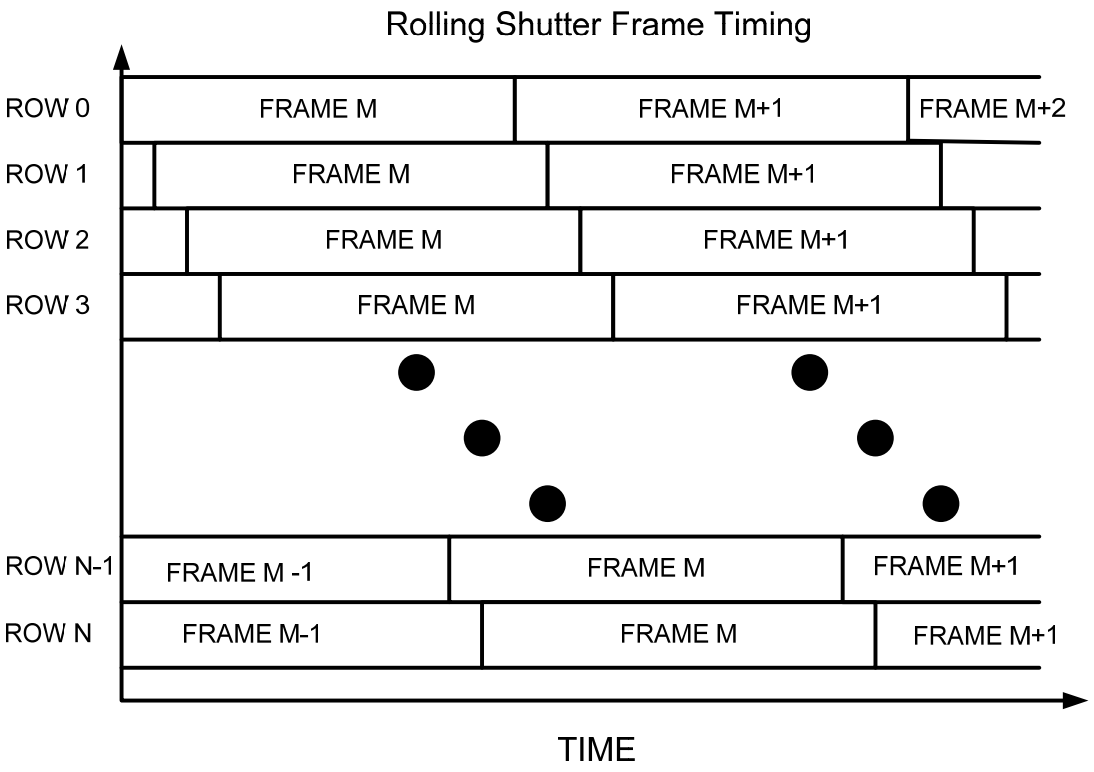
The CDS operation in Rolling Shutter mode is illustrated in Figure 10. The floating diffusion voltages of rows N-M, N-M+1, and N are shown. The reset sample for each row is S1 and the data sample for each row is S2. The final pixel value is the difference between S2 and S1.

Figure 10. CDS Operation in Rolling Shutter Mode



In Rolling Shutter readout, each row in the sensor integrates photo-charge for the same amount of time but the exact time interval is different. Moreover, the integration interval for row N+1 is shifted by one line time in comparison to row N. Figure 11 illustrates this effect.

Figure 11. Integration during Rolling Shutter Mode



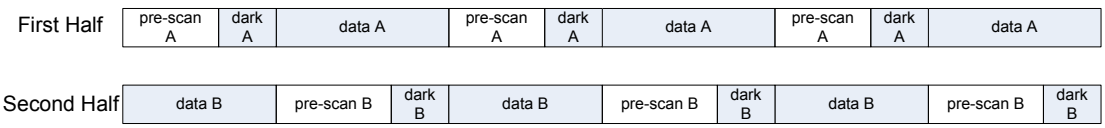
Seamless change of integration time in Rolling Shutter readout

Seamless change of integration time in Rolling Shutter readout mode is implemented on this sensor to allow standard auto exposure algorithms to be implemented in a camera. This operation is always active in Rolling Shutter readout mode. Seamless change of integration time is implemented in the sensor by forcing the integration time of each row in each frame to be the same. This enables smooth video output when integration time is used as an electronic shutter.

Pseudo single port readout mode

By programming the starting ROI address, the ending ROI address, enabling dark row operation and reset using the READ pin function, both halves of the sensor can be operated in tandem synchronously, behaving as if the sensor had only one output port. Data will be outputted from one output port while the other output port is generating pre-scan and dark row data as illustrated in the following diagram. Note that time is increasing from left to right in the diagram. The shaded regions are where F_VALID is asserted.

Figure 12. Pseudo single port readout timing



As illustrated in Figure 12, it is a requirement that the pre-scan and dark region of one half of the sensor must match the data region of the other half of the sensor for seamless synchronous operation. It is also required that one half of the sensor has Register 2 bit 22 equal to 0 (the

default) so the readout order for the frame is pre-scan rows / dark rows / active imager rows (“data”) while the other half of the sensor has Register 2 bit 22 equal to 1 so the readout order for the frame is active imager rows (“data”) / pre-scan rows / dark rows.

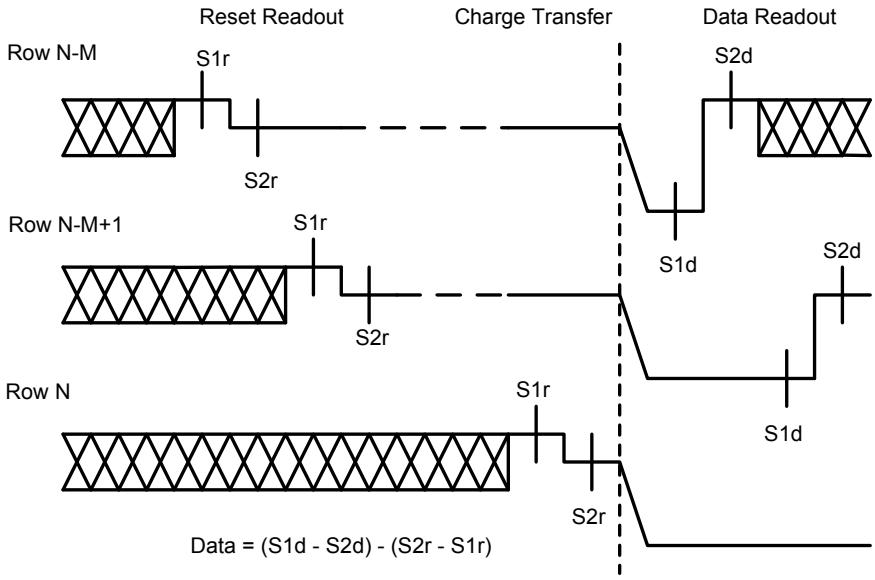
Global Shutter

Global Shutter operation allows every pixel in the sensor to integrate charge during the same time period. This minimizes motion artifacts when compared with Rolling Shutter operation. The CIS2521 performs Global Shutter using TX1 (transfer charge from pinned photodiode to floating diffusion) and TX2 (dump charge from pinned photodiode) to simultaneously control the end and start of integration respectively. Both TX1 and TX2 are active high, i.e. they transfer or dump charge when high.

In order to achieve low noise readout, correlated double sampling (CDS) must be performed to mitigate the effects of reset and 1/f noise in each pixel. Due to the global operation of TX1, the typical Rolling Shutter-type readout method (scrolling reset and then readout of each line) cannot be used to perform CDS. Therefore correlated quadruple sampling (CQS) is used to minimize read noise. CQS requires that the sensor be read out twice to construct each image frame. Moreover, a Reset frame and a Data frame are required for each image and the final image is created by subtracting the Reset frame from the Data frame. The first readout, i.e. the Reset frame, is a measurement of the kTC noise charge on the floating diffusion in each pixel. The second readout, i.e. the Data frame, is a measurement of the charge transferred from the pinned photodiode onto the floating diffusion.

Figure 13 illustrates the operation of CQS. S1r and S2r are reset samples collected during a Reset frame, and S1d and S2d are data samples collected during a Data frame. During a Reset frame each row within the ROI is read out sequentially. When a given row is selected all of the floating diffusion capacitances in that row are first hard reset to RD via the reset transistor in each pixel. Then, while the reset transistor is on, S1r samples the pixel voltage. Then the reset gate is turned off and S2r samples the floating diffusion, i.e. the noise charge. After all of the rows in the Reset frame are read out, charge can be transferred from the pinned photodiode to the floating diffusion capacitance in each pixel. After charge is transferred to the floating diffusion capacitance a Data frame can be collected. Similar to the readout of a Reset frame, a Data frame is read out sequentially row by row. While a given row is selected, all of the floating diffusion capacitances in that row are first sampled via S1d. Then the reset transistor in each pixel is turned on and S2d samples the pixel voltage. Finally the Reset frame is subtracted from the Data frame, external to the sensor, forming the image S1d-S2r. Note that this assumes that S1r and S2d are the same value, which is only true if RD is noiseless. Therefore, the noise voltage on RD is critical to the final read noise of the sensor in Global Shutter operation.

Figure 13. Correlated quadruple sampling operation



The following sections discuss Global Shutter operation in more detail and explain Reset frame and Data frame readout.

Reset frame readout

In Global Shutter mode, reset readout occurs when the DATA_SEL is low and the READ is high. Each Reset frame begins at the first row of ROI_1 and ends with the last row of ROI_2. For example, if ROI_1 start = 2047 and ROI_1 stop = 1080 then 952 pre-scan lines and 16 optically dark lines are sequentially read out from ROI_1. If ROI_2 start = 11 and ROI_2 stop = 1070 then the row counter counts up and 1060 active rows are read out of the sensor in ROI_2. Note that after row 1080 is read out of ROI_1 then the next row, i.e. the first row of ROI_2, is row 11. If DATA_SEL is held low and READ is held high, Reset frames will continue to be generated by the sensor and the row counter will continuously cycle through the row values in the current ROIs.

In video mode every Reset frame needs to be followed by a Data frame. Note that just like Rolling Shutter mode, the frame blanking time is determined by the number of pre-scan lines in each image. When switching between a Reset frame and a Data frame, DATA_SEL should be toggled during the frame blanking period.

Data frame readout

In Global Shutter mode, data readout occurs when the DATA_SEL is high and the READ is high. Each Data frame begins at the first row of ROI_1 and ends with the last row of ROI_2. For example, if ROI_1 start = 2047 and ROI_1 stop = 1080 then 952 pre-scan lines and 16 optically dark lines are sequentially read out from ROI_1. If ROI_2 start = 11 and ROI_2 stop = 1070 then the row counter counts up and 1060 active rows are read out of the sensor in ROI_2. Note that after row 1080 is read out of ROI_1 then the next row, i.e. the first row of ROI_2, is row 11. If DATA_SEL is held high and READ is held high, Data frames will continue to be generated by the sensor and the row counter will continuously cycle through the row values in the current ROIs. To perform correlated quadruple sampling, a Reset frame must be read out before each Data frame. When performing long integrations (greater than one frame time), multiple Reset frames may occur before a Data frame. For correct CQS sampling, the pair of frames chosen for CQS should be the Data frame and the Reset frame that occurs just before it.

Pause/Resume using READ pin

The READ pin switching to 0 will glitchlessly stop SCLK when JTAG Register 2 (mode register) bit 21 is 0, resulting in a “zero activity” pause operation. All sensor activities other than JTAG write or reset will be frozen. The assertion of the READ pin to 1 will cause SCLK to resume normal sensor operation. While the clock is stopped, it is possible that the voltage ramp generator will lose synch. The voltage ramp generator will take up to 65 row periods to stabilize.

Reset using READ pin

When JTAG Register 2 (mode register) bit 21 is 1, READ resets the sensor state (except the JTAG register values will not be forced back to their default values). This behavior is necessary to either:

a. start operation from a controlled start point, or
b. start synchronously for pseudo single port readout operation.

External trigger using READ pin

When JTAG Register 2, bit 23, is 1, it overrides the setting of bit 21 as described above and modifies the behavior of the READ pin. This is called external trigger mode. In this mode, the READ pin is sampled using the falling edge of CHARGE_TRANS. A change in the value of READ before and after the sample qualifies as a transition on READ.

Global Shutter external trigger

In this mode, each transition of the READ pin causes one and only one frame of either reset or data operation (depending on the value of DATA_SEL) before the sensor goes into an “idling” state where only one virtual row is continuously being accessed. In the “idling” state, the sensor is waiting for the next transition on READ. While the sensor is “idling”, external control signals TX1 and TX2 can be applied to precisely control the start and duration of the frame exposure. The response time of the sensor to a READ transition is one row time, i.e. the amount of time required to switch from the virtual row to a valid row.

Rolling Shutter external trigger

In this mode, each transition of the READ pin causes one and only one frame of either rolling reset or rolling read operation before the sensor goes into an “idling” state where only one virtual row is continuously accessed. Another JTAG bit, mode register bit 19, is added for further refinement.

If bit 19 is set to 0, when READ goes from 0 to 1, the complete region of interest (ROI1 if enabled and ROI2) goes through a rolling reset (no data is read). When READ goes to 0, the complete region of interest goes through a rolling data readout. The exposure then is the amount of time that READ is 1.

If bit 19 is set to 1, when READ has a transition, the complete region of interests (ROI1 if enabled and ROI2) goes through a rolling readout with an immediate reset on the same row. The amount of exposure is therefore approximately the duration of the READ pulse. Even though all rows have the same exposure time, the start of exposure differs from row to row. The last row of the frame starts exposure almost a frame time after the rising transition of READ.

TX2 can be used to address the exposure issue described in previous paragraph. When TX2 is asserted, the exposure is held off until the fall of TX2. This means all rows will have the same exposure start time but different exposure end time. This difference may not matter if the light source is pulsed.

Timing diagrams

Frame and line timing diagrams of the CIS2521 sensor in various operating modes are shown next.

Figure 14. Basic Rolling Shutter Mode

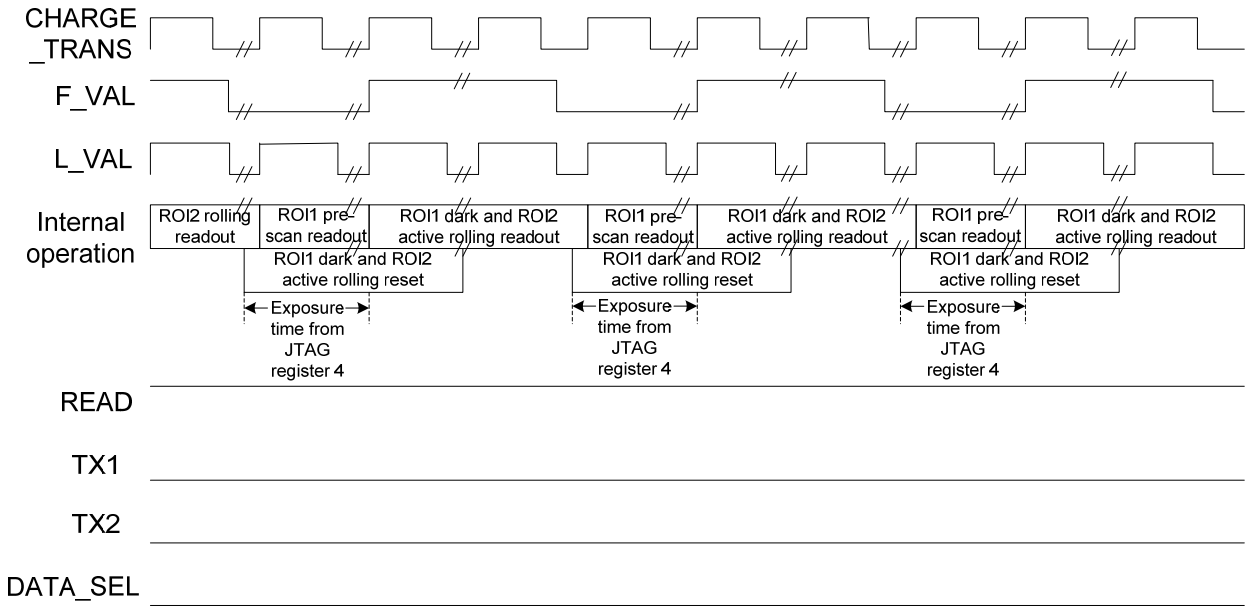


Figure 15. Rolling Shutter Mode using READ pin to extend exposure time, Reg 2 bit 21 = 0

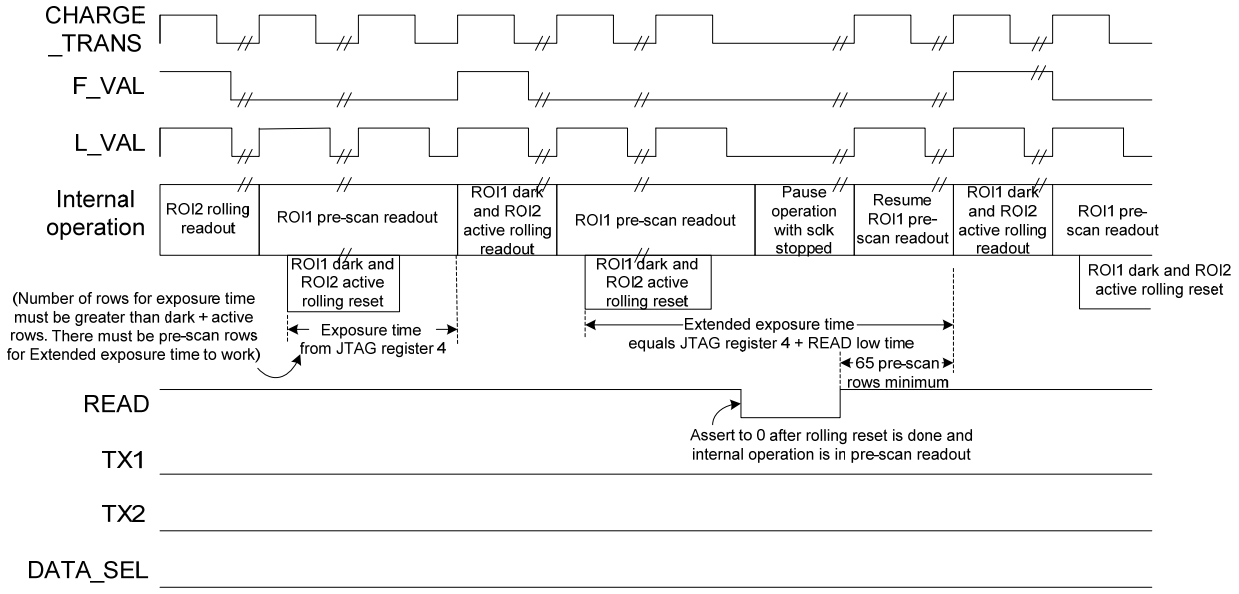


Figure 16. Basic Global Shutter Mode

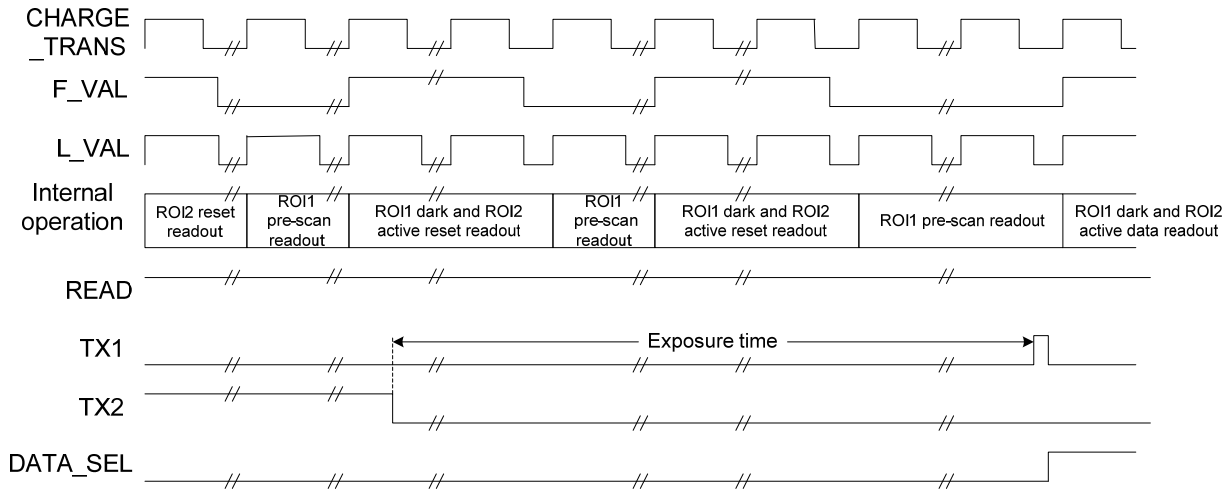
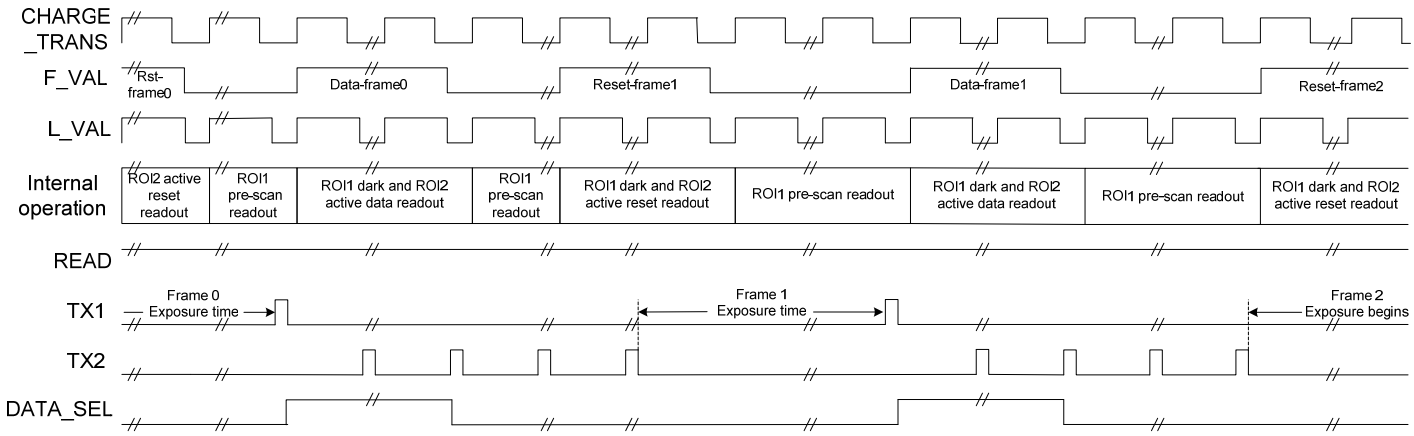


Figure 17. Basic Global Shutter Mode, Short Exposure (Similar to Fig 16 but with more details)



Note: Figures 17 and 18 show an identical readout mode (Basic Global Shutter Mode) with the only difference being that Figure 17 gives the example of a short exposure time and Figure 18 has a long exposure time.

The signals that are different are F_VAL (Figure 17 has one Reset frame preceding the Data frame, Figure 18 has two) and TX2 (Figure 17 has TX2 pulsed during the CHARGE_TRANS low period in each row readout, and Figure 18 has TX2 continuously on or continuously off).

Previously it has been stated that TX2 should be pulsed during the CHARGE_TRANS low time to avoid banding artifacts in the image. Since the Global Shutter final image is constructed from the Data frame and the immediately preceding Reset frame, any TX2 activity during this immediately preceding Reset frame must be pulsed, and this is shown in Figure 17.

In Figure 18, however, the last falling edge of TX2 is not in the immediately preceding Reset frame (Reset frame 1), but rather in the Reset frame before that (Reset frame 0). TX2 activity in

this region cannot induce any banding artifacts in the final Global Shutter image, since only data in the immediately preceding Reset frame (Reset frame 1) is used to create the final image.

Therefore, pulsing TX2 in Global Shutter is not necessary as long as there is no TX2 activity when active imager rows are being read out for a Data frame or its immediately preceding Reset frame. Having TX2 continuously on during either of these periods would produce banding artifacts. A time period when active imager rows are being read out roughly corresponds to when F_VAL is high, though F_VAL is high for both dark rows and active imager rows (= “physical rows”), and F_VAL (by default) has a 2 row time delay in its rise and fall times from when the physical rows begin and end their frame readout.

Of course, all complications can be avoided by pulsing TX2 during the CHARGE_TRANS low time regardless of the exposure time. However, pulsing TX2 incurs a cost in current consumption. In Low power applications, TX2 may therefore avoid pulsing for long exposure times, as is shown in Figure 18 below.

Figure 18. Basic Global Shutter Mode, Long Exposure (Similar to Fig 16 but with more details)

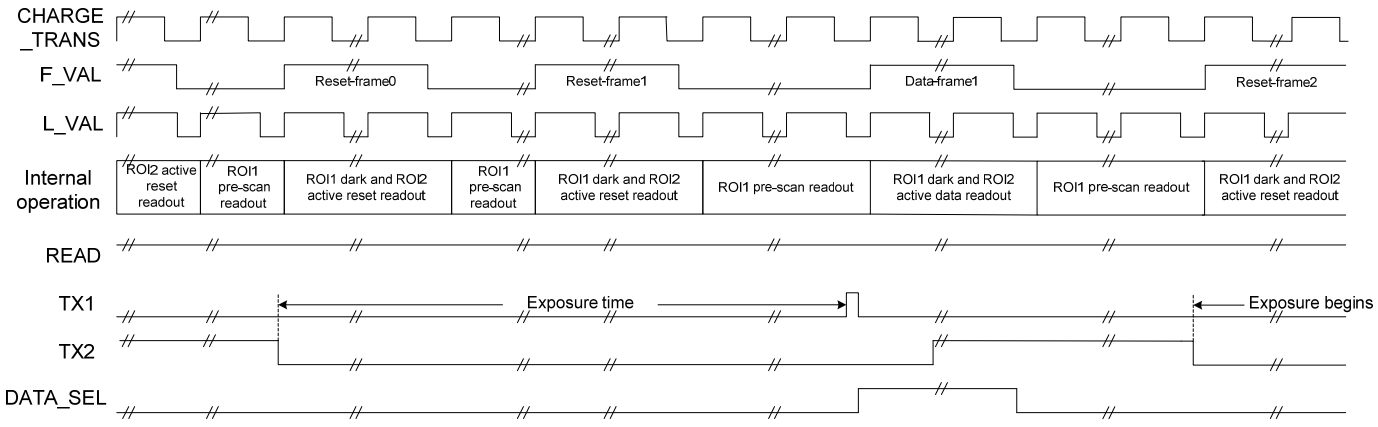


Figure 19. Global Shutter Mode using READ pin to extend exposure time

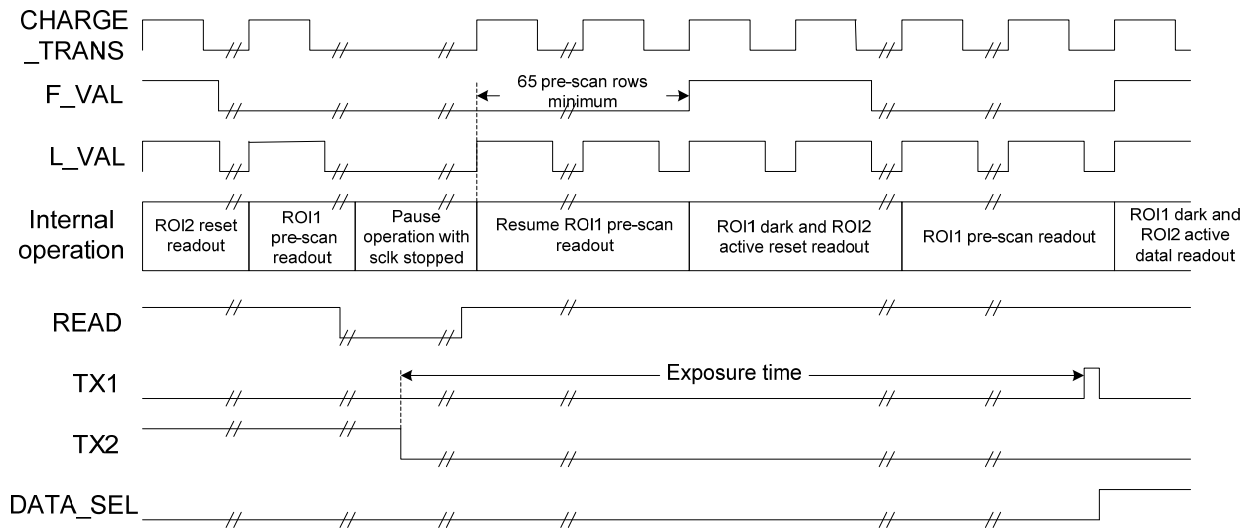
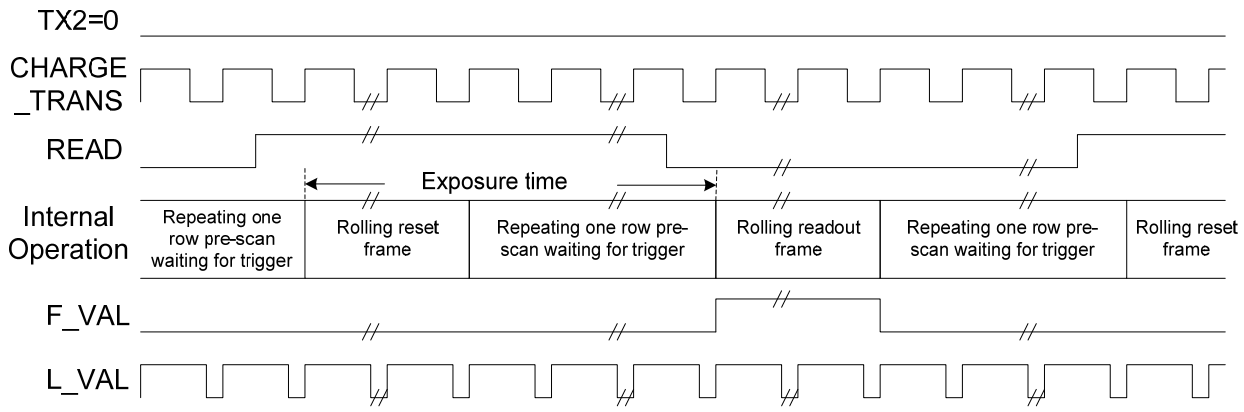


Figure 20. Rolling Shutter Mode with External Trigger, Reg 2 bit19=0 and bit23=1



Figures 20, 21, and 22 all use external trigger. In Figure 20, Rolling Shutter exposure is controlled by READ. In Figure 21, Rolling Shutter exposure is controlled by READ and TX2. In Figure 22, Global Shutter exposure is controlled by TX1 and TX2 pulses, as usual, but the timing of Reset and Data frame readouts is controlled by READ.

Figure 21. Rolling Shutter Mode with External Trigger, Reg 2 bit 19=1 and bit 23=1

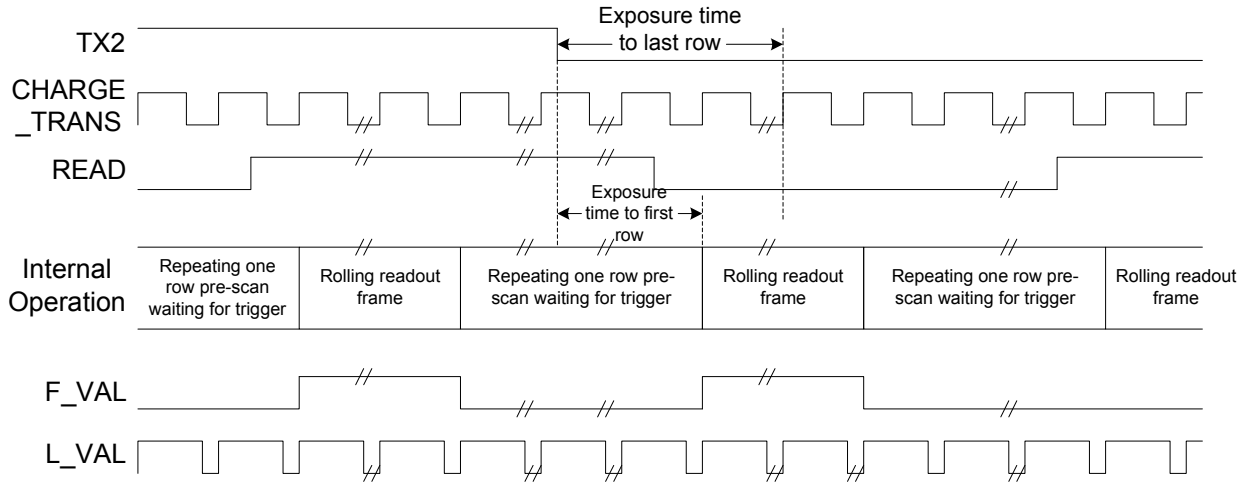
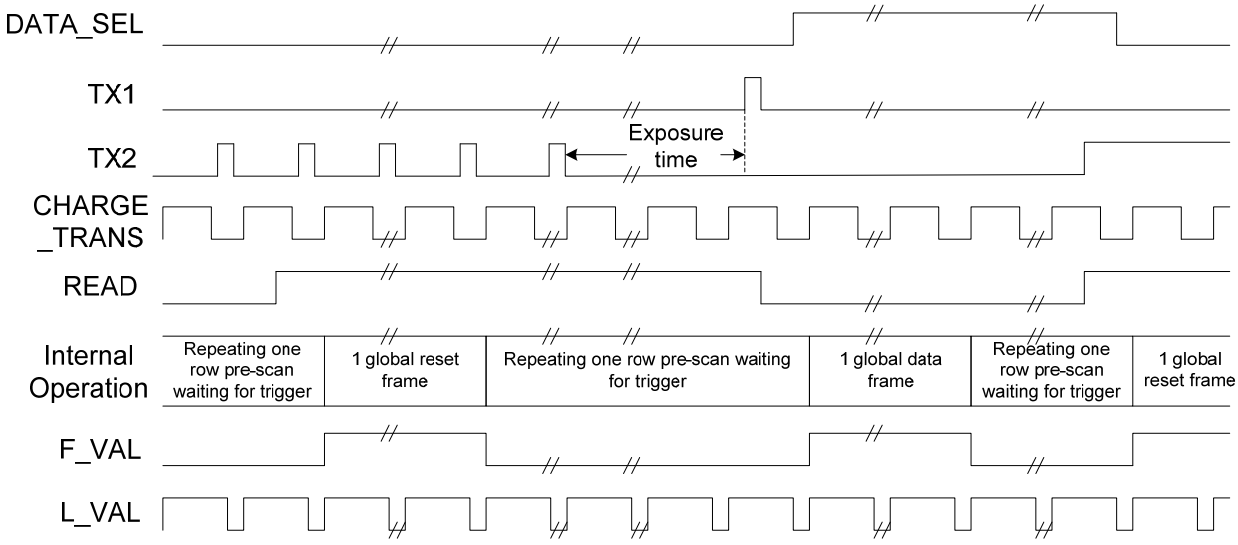


Figure 22. Global Shutter Mode with External Trigger



Note that in Figure 21 there is a transition in TX2 during a CHARGE_TRANS high period, and in Figure 22 there is a TX1 pulse during a CHARGE_TRANS high period. Normally this would be forbidden because an artifact might be induced. However, in both cases, the imager is reading out pre-scan rows at these times, and no image artifacts can result during pre-scan readout.

Packaging information

Standard Package drawings

All dimensions are in mm.

Figure 23. Top View of CIS2521 Standard Package

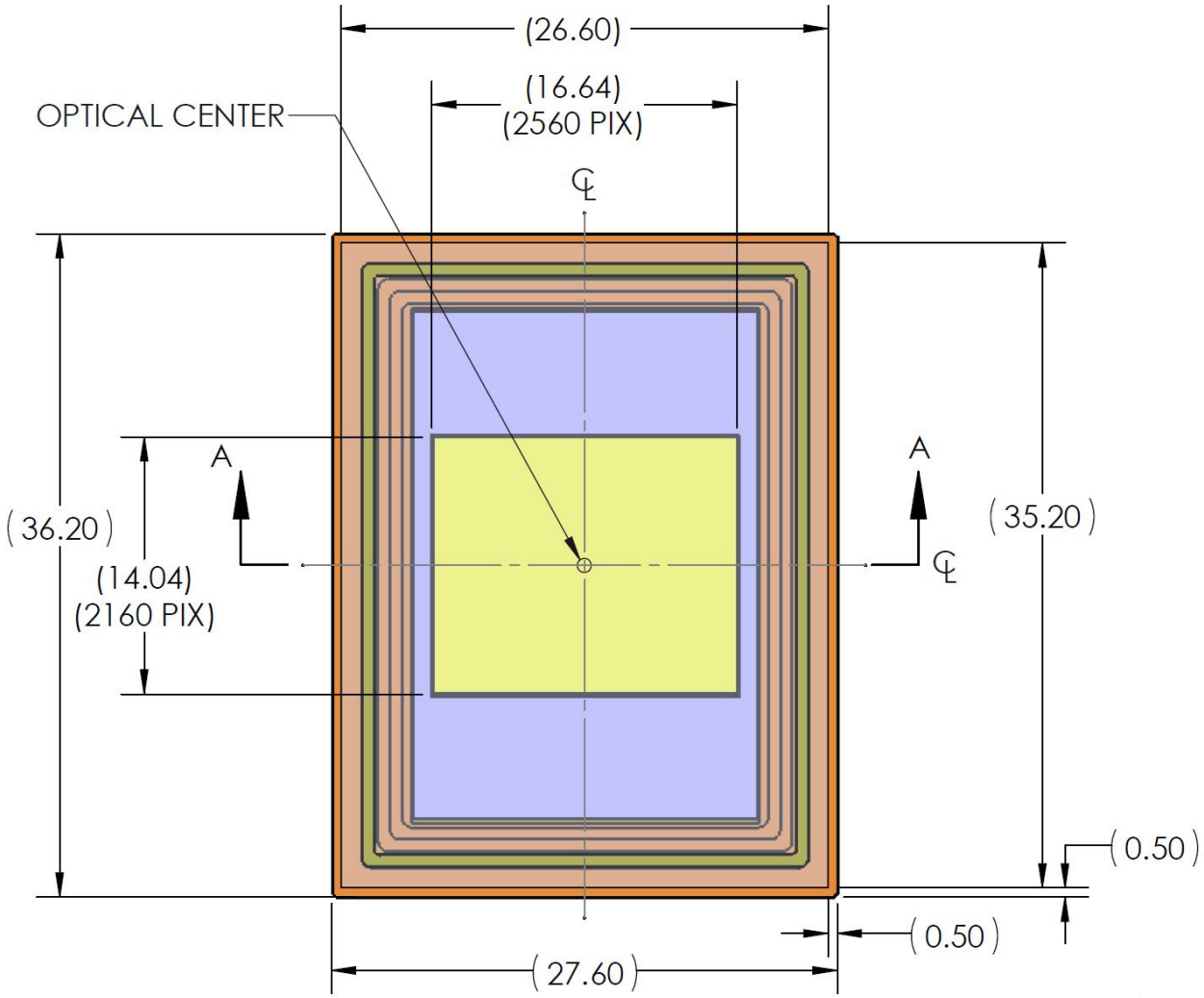


Figure 24. Side View of CIS2521 Standard Package

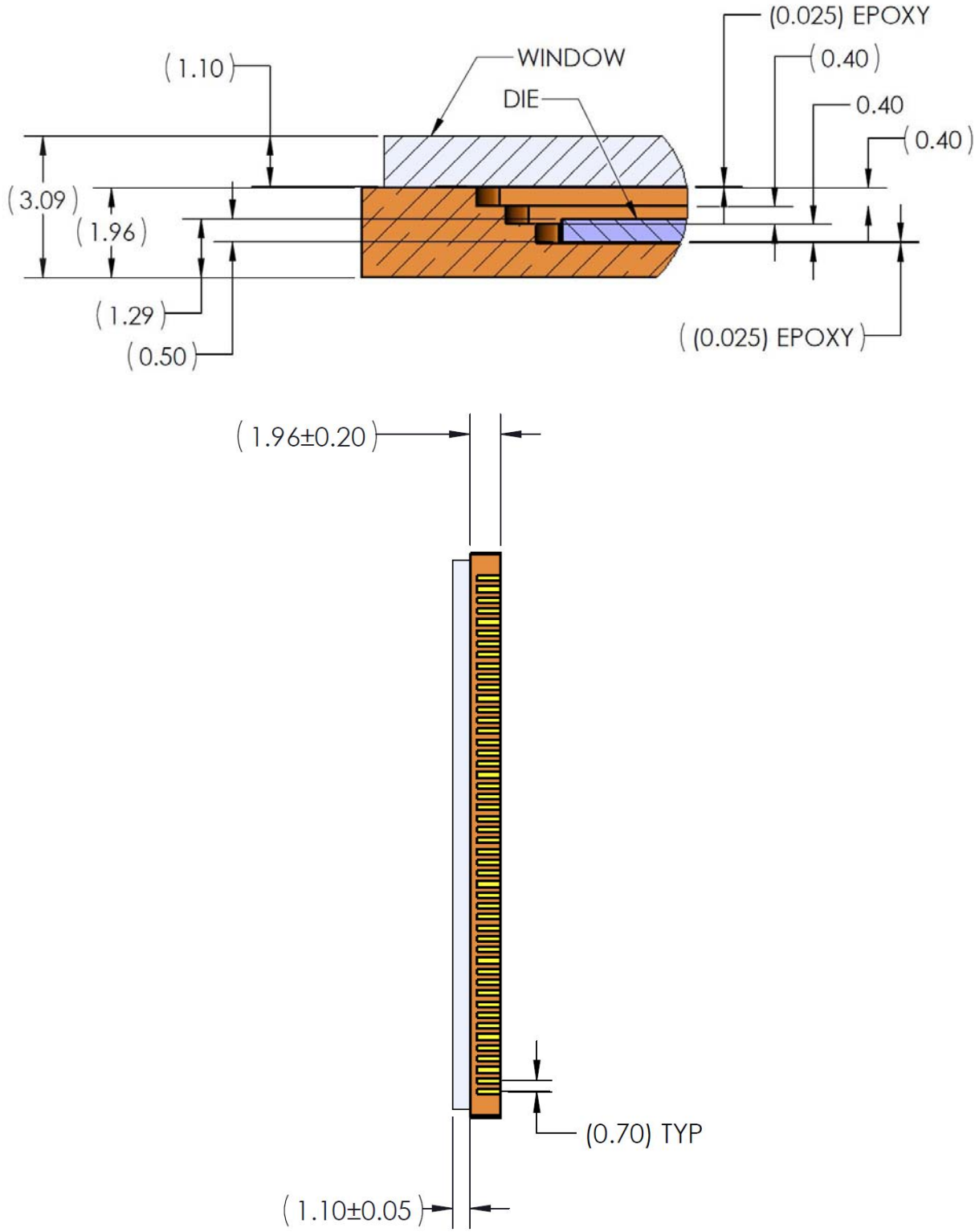
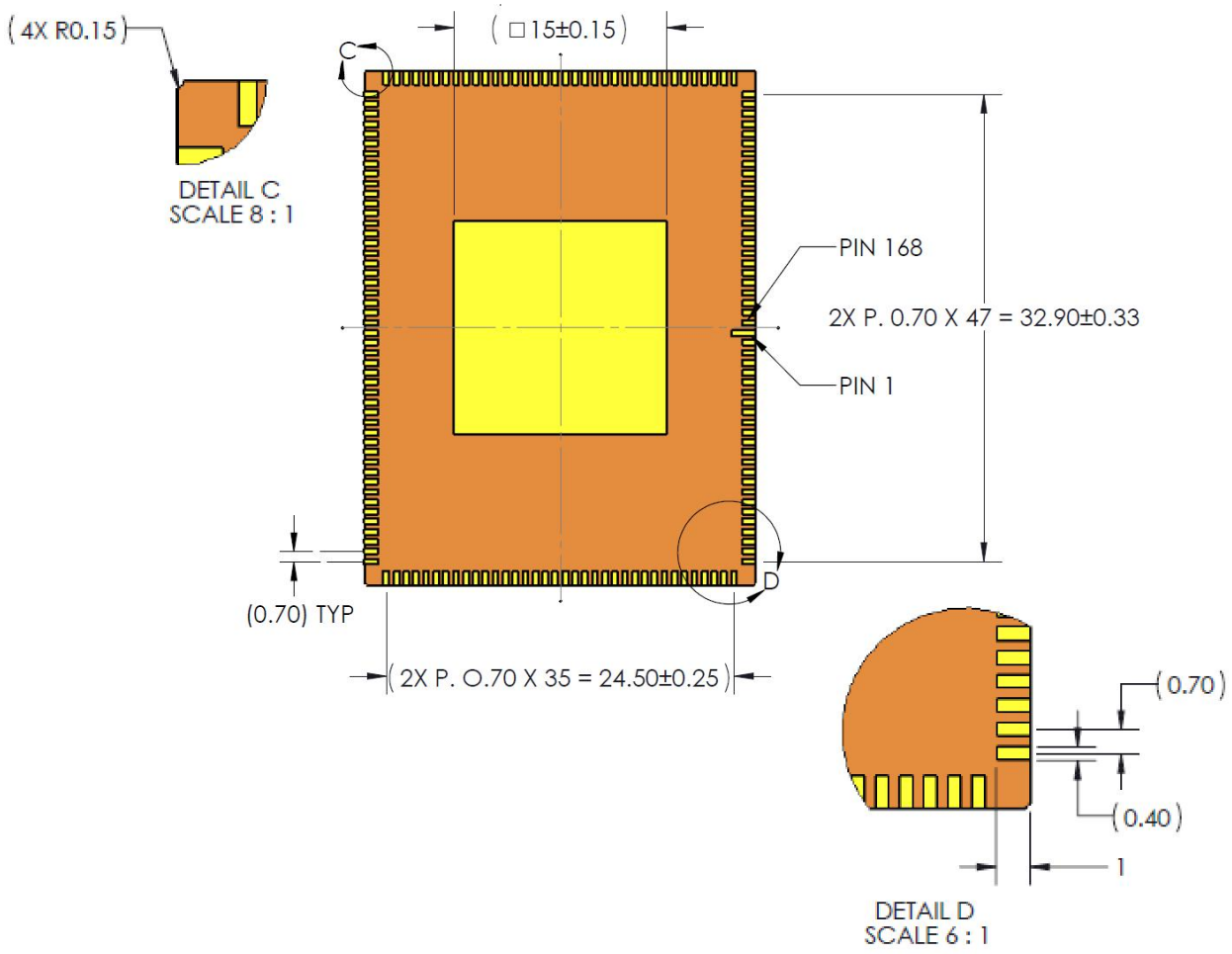


Figure 25. Bottom View of CIS2521 Standard Package



The standard package has a die placement spec (optical center of die to package center) of +/- 4 mils. The die rotation spec (relative to the package sides) is < 1°. The die tilt spec (relative to the package bottom) is < 1°.

The thermal pad at the bottom of the package should be grounded.

Scientific Package drawings

All dimensions are in mm.

Figure 26. Top View for CIS2521 Scientific Package

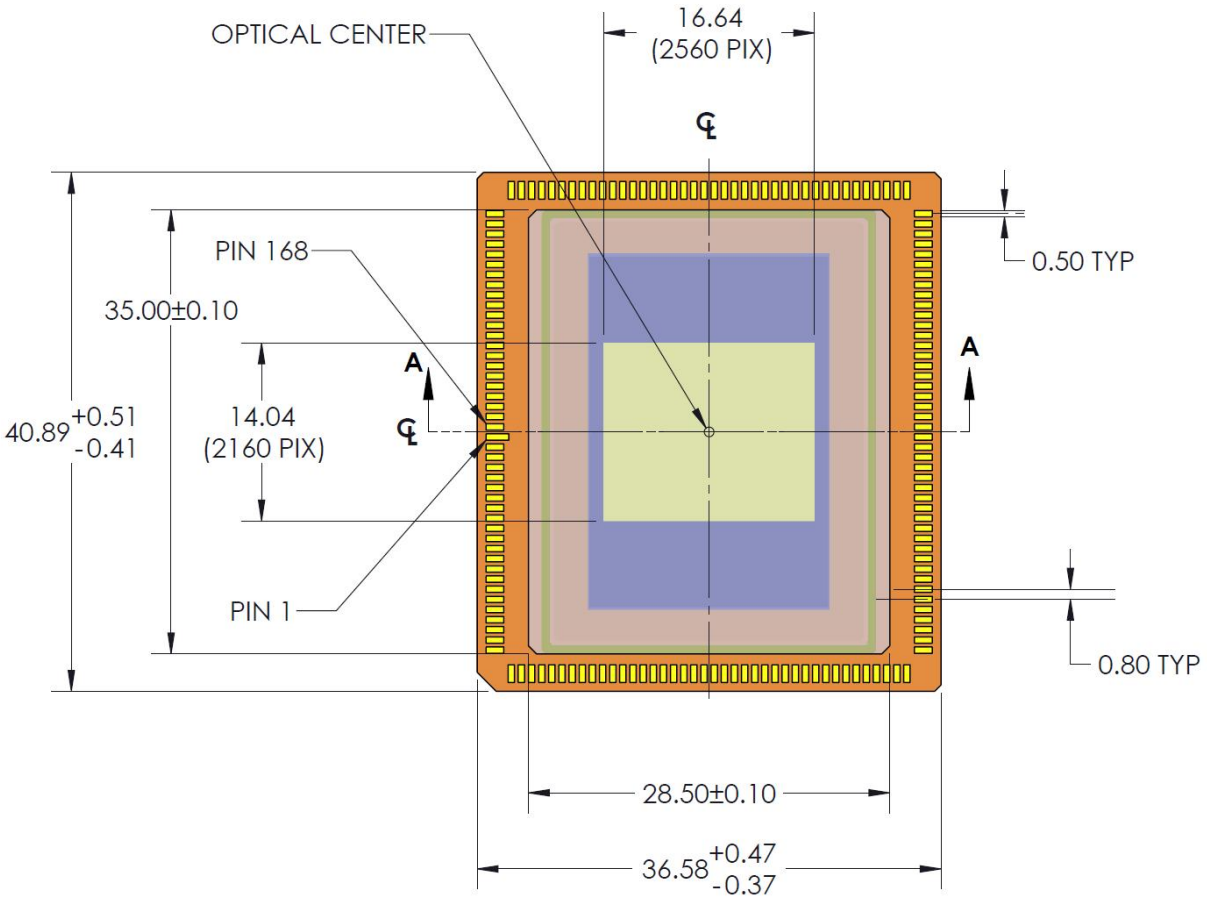


Figure 27. Side View of CIS2521 Scientific Package

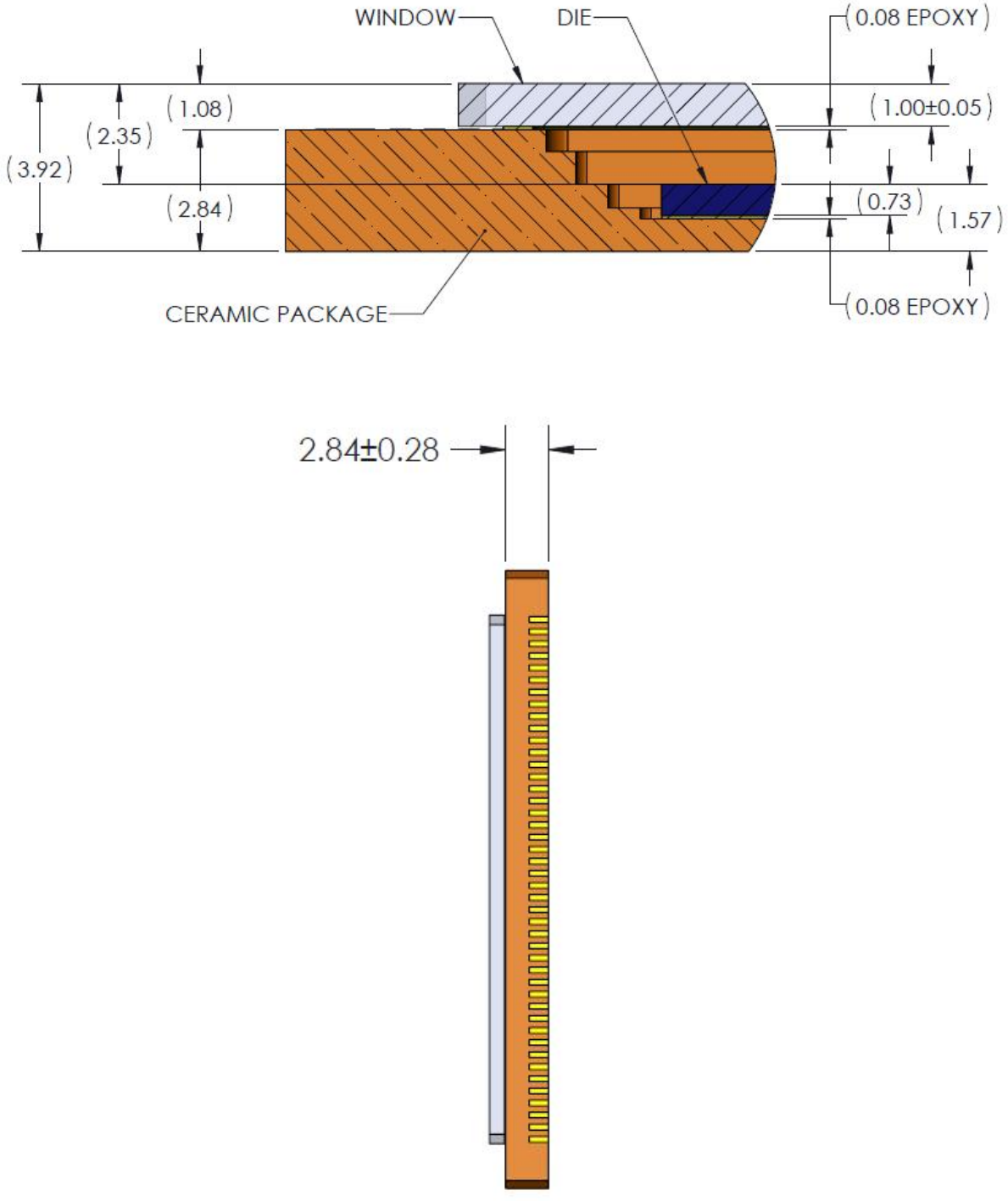
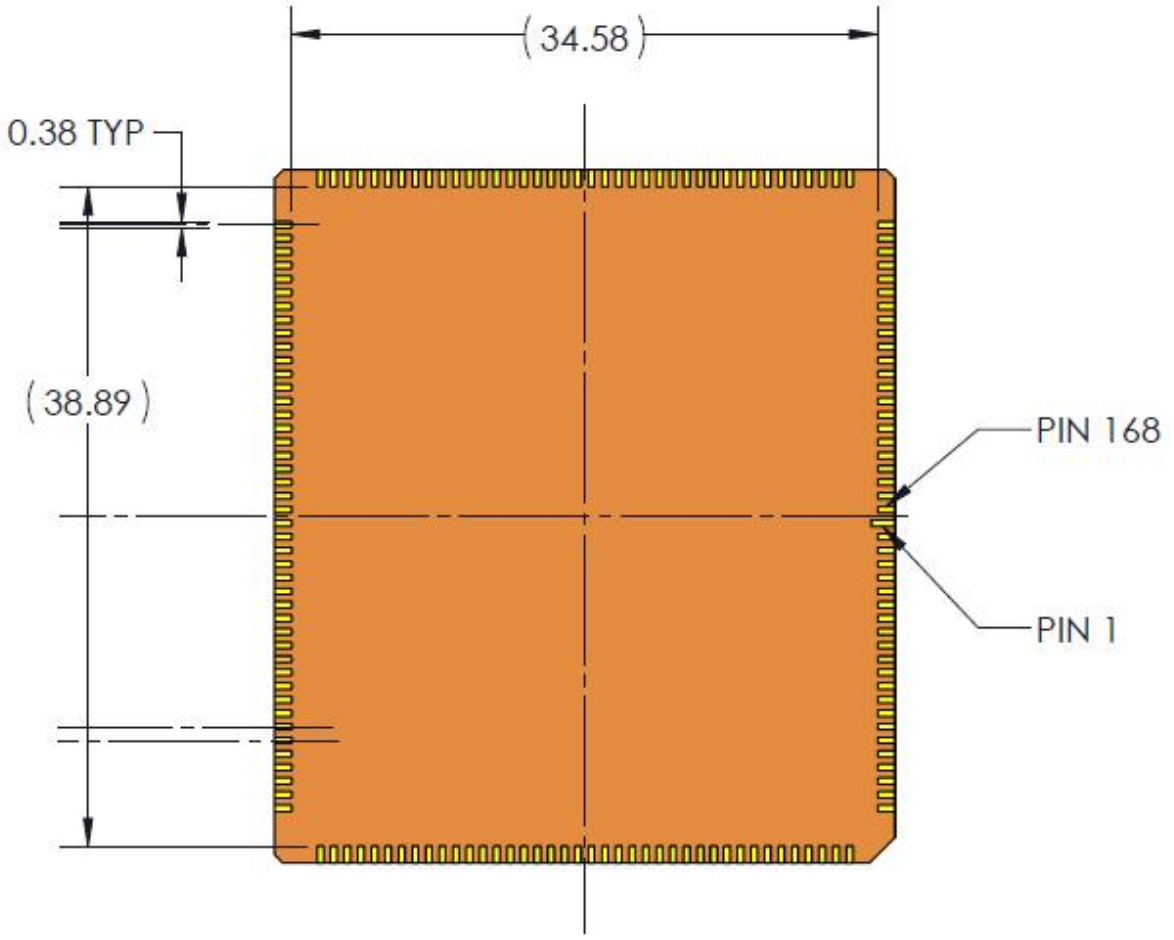


Figure 28. Bottom View of CIS2521 Scientific Package



The scientific package has a die placement spec (corners of die to package corner fiducials) of +/- 2.5 mils. The die rotation spec (relative to the package sides) is < 125 microns. The die tilt spec (relative to the package bottom) is < 125 microns.

Pin list for both Scientific and Standard packages

The CIS2521 image sensor is mounted in a 168-pin ceramic leadless chip carrier (LCC package) for both the Scientific and Standard packages. For both the package types, the pin list is identical. The list shown below provides a complete description of the pin names, their functions and electrical requirements. Note the suffix BT is appended to pins at the bottom of the sensor and the suffix TP is appended to pins at the top of the sensor, the suffix L is appended to pins on left side of the sensor, and the suffix R is appended to pins on right side of the sensor.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
1	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
2	VTX1_NEG_L	Supply		0~-1.5v/100mA 1µs pulse, Ripple < 100µV RMS	TX1 negative supply
3	AGND	Ground			AGND common ground 0V
4	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
5	AVDD_RST1_L	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST1 reset supply
6	DVDD_3V3_L	Supply		3.3v/1mA, Ripple < 1mV RMS	3.3V digital supply
7	AVDD_RST2_L	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
8	VTX2_NEG_L	Supply		+0.8~-1.5v/100mA 1µs pulse, Ripple < 1mV RMS	TX2 negative supply
9	AVDD_PIX_BT	Supply		3.3v/25mA, Ripple < 100µV RMS	Pixel source follower supply
10	AGND	Ground			AGND common ground 0V
11	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
12	AGND	Ground			AGND common ground 0V

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
13	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
14	TX2_BT	Input	1.8v hstl		Global TX2 Charge dump control for the bottom imager half. Rise/fall time < 500ns, Skew < 100ns, Ripple < 1mV RMS. (Typically this pin is only used during Global Shutter to provide the “Global TX2” charge dump pulse that marks the beginning of Global Shutter integration.)
15	TX1_BT	Input	1.8v hstl		Global TX1 Charge transfer control for the bottom imager half. Rise/fall time < 500ns, Skew < 100ns, Ripple < 100µV RMS. (Typically this pin is only used during Global Shutter to provide the “Global TX1” charge transfer pulse that marks the end of Global Shutter integration.)

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
16	DATA_SEL_BT	Input	1.8v hstl		DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used for sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly switching between 0 and 1.
17	AGND	Ground			AGND common ground 0V
18	READ_BT	Input	1.8v hstl		External start/pause readout activities control Input
19	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
20	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
21	COUNT_EN1_BT	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
22	COUNT_EN0_BT	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
23	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
24	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
25	CHARGE_ TRANS_BT	Output	1.8v hstl		Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL signals on external pins, and the timing of these signals should (usually) be correlated with CHARGE_TRANS (Note 2)
26	F_VALID_BT	Output	1.8v hstl		Frame valid Output. Pulses high once each frame when digital data for physical rows (i.e. dark and active imager but not pre-scan rows) appears on the DOUT/DOUT_LG pins. F_VALID rising and falling edges are controlled by the wavetable. Also called FVAL.
27	L_VALID_BT	Output	1.8v hstl		Line valid Output. Pulses once during each line readout regardless of the type of line being read out (pre-scan / dark / active imager). L_VALID rising and falling edges are controlled by the wavetable. Also called LVAL.
28	AGND	Ground			AGND common ground 0V
29	DOUT_LG0_BT	Output	1.8v hstl		Low gain ADC Output bit 0. DOUT_LG[10:0]_BT data is in Gray code.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
30	DOUT0_BT	Output	1.8v hstl		High gain ADC Output bit 0. DOUT[10:0]_BT data is in Gray code.
31	DOUT_LG2_BT	Output	1.8v hstl		Low gain ADC Output bit 2. DOUT_LG[10:0]_BT data is in Gray code.
32	DOUT2_BT	Output	1.8v hstl		High gain ADC Output bit 2. DOUT[10:0]_BT data is in Gray code.
33	AGND	Ground			AGND common ground 0V
34	DOUT_LG4_BT	Output	1.8v hstl		Low gain ADC Output bit 4. DOUT_LG[10:0]_BT data is in Gray code.
35	DOUT4_BT	Output	1.8v hstl		High gain ADC Output bit 4. DOUT[10:0]_BT data is in Gray code.
36	DOUT_LG6_BT	Output	1.8v hstl		Low gain ADC Output bit 6. DOUT_LG[10:0]_BT data is in Gray code.
37	DOUT6_BT	Output	1.8v hstl		High gain ADC Output bit 6. DOUT[10:0]_BT data is in Gray code.
38	AGND	Ground			AGND common ground 0V
39	DOUT_LG8_BT	Output	1.8v hstl		Low gain ADC Output bit 8. DOUT_LG[10:0]_BT data is in Gray code.
40	DOUT8_BT	Output	1.8v hstl		High gain ADC Output bit 8. DOUT[10:0]_BT data is in Gray code.
41	DOUT_LG10_BT	Output	1.8v hstl		Low gain ADC Output bit 10. DOUT_LG[10:0]_BT data is in Gray code.
42	DOUT10_BT	Output	1.8v hstl		High gain ADC Output bit 10. DOUT[10:0]_BT data is in Gray code.
43	AGND	Ground			AGND common ground 0V
44	SCLK_BT	Input	1.8v hstl		System clock. Input frequency between 30 MHz and 287 MHz is acceptable. Operation below 30 MHz is not recommended as the internal VRAMP voltage may become nonlinear.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
45	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
46	CLK_OUT_BT	Output	1.8v hstl		Clock to synchronize the data Output
47	AGND	Ground			AGND common ground 0V
48	DOUT9_BT	Output	1.8v hstl		High gain ADC Output bit 9. DOUT[10:0]_BT data is in Gray code.
49	DOUT_LG9_BT	Output	1.8v hstl		Low gain ADC Output bit 9. DOUT_LG[10:0]_BT data is in Gray code.
50	DOUT7_BT	Output	1.8v hstl		High gain ADC Output bit 7. DOUT[10:0]_BT data is in Gray code.
51	DOUT_LG7_BT	Output	1.8v hstl		Low gain ADC Output bit 7. DOUT_LG[10:0]_BT data is in Gray code.
52	AGND	Ground			AGND common ground 0V
53	DOUT5_BT	Output	1.8v hstl		High gain ADC Output bit 5. DOUT[10:0]_BT data is in Gray code.
54	DOUT_LG5_BT	Output	1.8v hstl		Low gain ADC Output bit 5. DOUT_LG[10:0]_BT data is in Gray code.
55	DOUT3_BT	Output	1.8v hstl		High gain ADC Output bit 3. DOUT[10:0]_BT data is in Gray code.
56	DOUT_LG3_BT	Output	1.8v hstl		Low gain ADC Output bit 3. DOUT_LG[10:0]_BT data is in Gray code.
57	AGND	Ground			AGND common ground 0V
58	DOUT1_BT	Output	1.8v hstl		High gain ADC Output bit 1. DOUT[10:0]_BT data is in Gray code.
59	DOUT_LG1_BT	Output	1.8v hstl		Low gain ADC Output bit 1. DOUT_LG[10:0]_BT data is in Gray code.
60	Reserved	Output	1.8v hstl		Output fixed at 0 Volts
61	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
62	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
63	RESETB_BT	Input	1.8v lvcmos		Active low reset Input
64	AGND	Ground			AGND common ground 0V
65	TMS_BT	Input	1.8v lvcmos		JTAG mode select control
66	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
67	TRSTB_BT	Input	1.8v lvcmos		JTAG reset (active low)
68	TDI_BT	Input	1.8v lvcmos		JTAG serial data Input
69	TCK_BT	Input	1.8v lvcmos		JTAG clock (should be less than 25 MHz)
70	AGND	Ground			AGND common ground 0V
71	TDO_BT	Output	1.8v hstl		JTAG serial data Output
72	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
73	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
74	VPTAT_BT	Output	Analog		Temperature sensor Output (Note 3)
75	RTRIM_BT	Output	Analog		External current reference resistor pad. Should have a 12.28 KΩ resistor connected to this pad at one end and ground at the other.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
76	EXT_VRAMP_BT	Input	Analog		Optional external VRAMP input that is used in place of the internal voltage ramp when JTAG Register 2 bit 16 = 1. Normally the internal VRAMP is used and this pin is either left as a no connection or tied to ground. If it is used, the ADC ramp power requirements are: voltage (from 1.0V to 2.5V) current (20mA)
77	AVDD_PIX_BT	Supply		3.3v/25mA, Ripple < 100µV RMS	Pixel source follower supply
78	VTX2_NEG_R	Supply		+0.8~-1.5v/100mA 1µs pulse, Ripple < 1mV RMS	TX2 negative supply
79	AVDD_RST2_R	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
80	DVDD_3V3_R	Supply		3.3v/1mA, Ripple < 1mV RMS	3.3V digital supply
81	AVDD_RST1_R	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST1 reset supply
82	AGND	Ground			AGND common ground 0V
83	VTX1_NEG_R	Supply		0~-1.5v/100mA 1µs pulse, Ripple < 100µV RMS	TX1 negative supply
84	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
85	AGND	Ground			AGND common ground 0V
86	VTX1_POS_R	Supply		3.3v/100mA 1µs pulse, Ripple < 1mV RMS	TX1 positive supply
87	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
88	AVDD_RST1_R	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST1 reset supply
89	DVDD_3V3_R	Supply		3.3v/1mA, Ripple < 1mV RMS	3.3V digital supply
90	AVDD_RST2_R	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
91	VTX2_POS_R	Supply		3.3v/100mA 1µs pulse, Ripple < 1mV RMS	TX2 positive supply
92	AGND	Ground			AGND common ground 0V
93	AVDD_PIX_TP	Supply		3.3v/25mA, Ripple < 100µV RMS	Pixel source follower supply
94	EXT_VRAMP_TP	Input	Analog		Optional external VRAMP input that is used in place of the internal voltage ramp when JTAG Register 2 bit 16 = 1. Normally the internal VRAMP is used and this pin is either left as a no connection or tied to ground. If it is used, the ADC ramp power requirements are: voltage (from 1.0V to 2.5V) current (20mA)
95	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
96	RTRIM_TP	Output	Analog		External current reference resistor pad. Should have a 12.28 KΩ resistor connected to this pad at one end and ground at the other.
97	VPTAT_TP	Output	Analog		Temperature sensor Output (Note 3)
98	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
99	TDO_TP	Output	1.8v hstl		JTAG serial data Output
100	TCK_TP	Input	1.8v lvcmos		JTAG clock (should be less than 25 MHz)

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
101	TDI_TP	Input	1.8v lvcmos		JTAG serial data Input
102	TRSTB_TP	Input	1.8v lvcmos		JTAG reset (active low)
103	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
104	TMS_TP	Input	1.8v lvcmos		JTAG mode select control
105	AGND	Ground			AGND common ground 0V
106	RESETB_TP	Input	1.8v lvcmos		Active low reset Input
107	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
108	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
109	Reserved	Output	1.8v hstl		Output fixed at 0 Volts
110	DOUT_LG1_TP	Output	1.8v hstl		Low gain ADC Output bit 1. DOUT_LG[10:0]_TP data is in Gray code.
111	DOUT1_TP	Output	1.8v hstl		High gain ADC Output bit 1. DOUT[10:0]_TP data is in Gray code.
112	AGND	Ground			AGND common ground 0V
113	DOUT_LG3_TP	Output	1.8v hstl		Low gain ADC Output bit 3. DOUT_LG[10:0]_TP data is in Gray code.
114	DOUT3_TP	Output	1.8v hstl		High gain ADC Output bit 3. DOUT[10:0]_TP data is in Gray code.
115	DOUT_LG5_TP	Output	1.8v hstl		Low gain ADC Output bit 5. DOUT_LG[10:0]_TP data is in Gray code.
116	DOUT5_TP	Output	1.8v hstl		High gain ADC Output bit 5. DOUT[10:0]_TP data is in Gray code.
117	AGND	Ground			AGND common ground 0V

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
118	DOUT_LG7_TP	Output	1.8v hstl		Low gain ADC Output bit 7. DOUT_LG[10:0]_TP data is in Gray code.
119	DOUT7_TP	Output	1.8v hstl		High gain ADC Output bit 7. DOUT[10:0]_TP data is in Gray code.
120	DOUT_LG9_TP	Output	1.8v hstl		Low gain ADC Output bit 9. DOUT_LG[10:0]_TP data is in Gray code.
121	DOUT9_TP	Output	1.8v hstl		High gain ADC Output bit 9. DOUT[10:0]_TP data is in Gray code.
122	AGND	Ground			AGND common ground 0V
123	CLK_OUT_TP	Output	1.8v hstl		Clock to synchronize the data Output.
124	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
125	SCLK_TP	Input	1.8v hstl		System clock. Input frequency between 30 MHz and 287 MHz is acceptable. Operation below 30 MHz is not recommended as the internal VRAMP voltage may become nonlinear.
126	AGND	Ground			AGND common ground 0V
127	DOUT10_TP	Output	1.8v hstl		High gain ADC Output bit 10. DOUT[10:0]_TP data is in Gray code.
128	DOUT_LG10_TP	Output	1.8v hstl		Low gain ADC Output bit 10. DOUT_LG[10:0]_TP data is in Gray code.
129	DOUT8_TP	Output	1.8v hstl		High gain ADC Output bit 8. DOUT[10:0]_TP data is in Gray code.
130	DOUT_LG8_TP	Output	1.8v hstl		Low gain ADC Output bit 8. DOUT_LG[10:0]_TP data is in Gray code.
131	AGND	Ground			AGND common ground 0V
132	DOUT6_TP	Output	1.8v hstl		High gain ADC Output bit 6. DOUT[10:0]_TP data is in Gray code.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
133	DOUT_LG6_TP	Output	1.8v hstl		Low gain ADC Output bit 6. DOUT_LG[10:0]_TP data is in Gray code.
134	DOUT4_TP	Output	1.8v hstl		High gain ADC Output bit 4. DOUT[10:0]_TP data is in Gray code.
135	DOUT_LG4_TP	Output	1.8v hstl		Low gain ADC Output bit 4. DOUT_LG[10:0]_TP data is in Gray code.
136	AGND	Ground			AGND common ground 0V
137	DOUT2_TP	Output	1.8v hstl		High gain ADC Output bit 2. DOUT[10:0]_TP data is in Gray code.
138	DOUT_LG2_TP	Output	1.8v hstl		Low gain ADC Output bit 2. DOUT_LG[10:0]_TP data is in Gray code.
139	DOUT0_TP	Output	1.8v hstl		High gain ADC Output bit 0. DOUT[10:0]_TP data is in Gray code.
140	DOUT_LG0_TP	Output	1.8v hstl		Low gain ADC Output bit 0. DOUT_LG[10:0]_TP data is in Gray code.
141	AGND	Ground			AGND common ground 0V
142	L_VALID_TP	Output	1.8v hstl		Line valid Output. Pulses once during each line readout regardless of the type of line being read out (pre-scan / dark / active imager). L_VALID rising and falling edges are controlled by the wavetable. Also called LVAL.
143	F_VALID_TP	Output	1.8v hstl		Frame valid Output. Pulses high once each frame when digital data for physical rows (i.e. dark and active imager but not pre-scan rows) appears on the DOUT/DOUT_LG pins. F_VALID rising and falling edges are controlled by the wavetable. Also called FVAL.

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
144	CHARGE_ TRANS_TP	Output	1.8v hstl		Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL signals on external pins, and the timing of these signals should (usually) be correlated with CHARGE_TRANS (Note 2)
145	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
146	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
147	COUNT_EN0_TP	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
148	COUNT_EN1_TP	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
149	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
150	DVDD_IO	Supply		1.8v/270mA @287MHz, Ripple < 25mV RMS	DVDD digital I/O supply
151	READ_TP	Input	1.8v hstl		External start/pause readout activities control Input
152	AGND	Ground			AGND common ground 0V

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
153	DATA_SEL_TP	Input	1.8v hstl		DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used fro sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly switching between 0 and 1.
154	TX1_TP	Input	1.8v hstl		Global TX1 Charge transfer control for the top imager half. Rise/fall time < 500ns, Skew < 100ns, Ripple < 100µV RMS. (Typically this pin is only used during Global Shutter to provide the “Global TX1” charge transfer pulse that marks the end of Global Shutter integration.)
155	TX2_TP	Input	1.8v hstl		Global TX2 Charge dump control for the top imager half. Rise/fall time < 500ns, Skew < 100ns, Ripple < 1mV RMS. (Typically this pin is only used during Global Shutter to provide the “Global TX2” charge dump pulse that marks the beginning of Global Shutter integration.)

Pin number	Pin name	Pin type	Signal type	Power requirements (Note 1)	Pin Description
156	DVDD	Supply		1.8v/290mA @287MHz, Ripple < 25mV RMS	DVDD digital core supply
157	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
158	AGND	Ground			AGND common ground 0V
159	AVDD_PIX_TP	Supply		3.3v/25mA, Ripple < 100µV RMS	Pixel source follower supply
160	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply
161	AGND	Ground			AGND common ground 0V
162	VTX2_POS_L	Supply		3.3v/100mA 1µs pulse, Ripple < 1mV RMS	TX2 positive supply
163	AVDD_RST2_L	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
164	DVDD_3V3_L	Supply		3.3v/1mA, Ripple < 1mV RMS	3.3V digital supply
165	AVDD_RST1_L	Supply		2.7v-3.0v/1mA, Ripple < 10µV RMS	AVDD_RST1 reset supply
166	VTX1_POS_L	Supply		3.3v/100mA 1µs pulse, Ripple < 1mV RMS	TX1 positive supply
167	AGND	Ground			AGND common ground 0V
168	AVDD	Supply		3.3v/270mA, Ripple < 1mV RMS	AVDD analog supply

Note 1: Power requirements are quoted with current values for the whole imager, not just the top or the bottom half, or the left or the right side.
Note that the most of the power requirement for the chip (< 2 Watts) comes from just 4 pins:

Name	Voltage	Current	Power requirement
DVDD	1.8 Volts	290 mA (@287 MHz)	522 mW (@ 287 MHz)
DVDD_IO	1.8 Volts	270 mA (@287 MHz)	486 mW (@ 287 MHz)
AVDD	3.3 Volts	270 mA	891 mW
AVDD_PIX	3.3 Volts	25 mA	82.5 mW

Just these four pins create a power requirement of 1981.5 mW (@287 MHz). The analog supplies to the chip are invariant with SCLK frequency, but the digital supplies (DVDD and DVDD_IO) have their current consumption scale linearly with frequency. Example: at ½ the peak SCLK frequency (143.5 MHz), DVDD would need 145 mA and DVDD_IO would need 135 mA.

Note that the power supplies with the tightest voltage ripple requirements are the ones closest to the pixel floating diffusion. RST1 and RST2 directly connect to the floating diffusion, so they have the tightest specs: less than 10 µV. VTX1_NEG and AVDD_PIX (which powers the Source Follower transistor on the pixel) are next at less than 100 µV ripple. VTX2_POS, VTX2_NEG, and VTX1_POS allow for the most (for voltages that touch the pixel) with a ripple voltage spec of less than 1 mV. (TX2 is further from the floating diffusion than TX1, and TX1 spends most of its time with VTX1_NEG on the TX1 gate, so that is the more critical of the TX1 voltages. The idea is to prevent power supply noise from capacitively coupling to the pixel floating diffusion.

Note 2: CHARGE_TRANS is an output provided by the wavetable that pulses once each row readout. For the default and BAE-recommended wavetables (see CIS2521 Programming Manual), the time to read out a row of pixels is equal to 2624 SCLKs. CHARGE_TRANS is high for 2319 SCLKs and low for 305 SCLKs. At full speed (287 MHz) this means that CHARGE_TRANS is low for 1.06 µseconds.

The CHARGE_TRANS signal does not directly control anything. It is a marker signal for the user to indicate when data sampling is occurring. When CHARGE_TRANS is high, data sampling of the pixel floating diffusion node voltage is occurring, or will shortly occur, or has recently occurred. When CHARGE_TRANS is low, data sampling of the pixel floating diffusion node voltage has already taken place and is in no danger of being disturbed

This is relevant in Global Shutter, because, unlike Rolling Shutter, the user must define the exposure time by inputting voltage pulses on the chip's external pins for TX1 and TX2. A pulse on TX2 marks the beginning of integration (because it clears out the pixel photodiode charge) while a pulse on TX1 marks the end of integration (because it transfers the pixel photodiode charge to the floating diffusion node to be read out).

These pulses go directly to the pixel, and therefore should occur during the CHARGE_TRANS low period when such pulses will not disturb the floating diffusion voltage sampling (because it has already occurred). Even at the highest speed, a 1 microsecond long TX1 or TX2 pulse is sufficient in duration to accomplish the necessary charge transfer. If the user fails to do this, the row of data that sees a TX1 or TX2 voltage transition during the CHARGE_TRANS high period will be corrupted.

There is one exception to this: it is not necessary to limit transitions in the TX1 or TX2 signals to the CHARGE_TRANS low period if the circumstances allow the user to be indifferent to whether the row of pixel data is corrupted. For example, if the row being read out is a pre-scan row, the TX1 and TX2 will not be connected to any physical row of pixels, and so interference of floating diffusion node voltages is not a concern. Figures 21 and 22 in this datasheet are examples of this. Another example is when Global Shutter is set up to loop on multiple reset frames prior to reading out the data frame in order to get an extended exposure time. In this case, the start of the integration period (indicated by a TX2 pulse) could be during a CHARGE_TRANS high period if it occurred during any of the Reset frames except the one that immediately precedes the Data frame. This is because the final image will be constructed from the Data frame and its immediately preceding Reset frame. If a line of data was corrupted in one of the earlier Reset frames, it makes no difference since that data will not be used to construct the final image. This consideration is also at work when, instead of pulsing the TX2, the user decides to hold TX2 high and mark the start of integration by dropping TX2. This is seen in Figures 16 and 18. In those figures, the TX2 signal goes from high to low much earlier than the Reset frame that immediately precedes the Data frame, and so there is no risk of inducing artifacts in the final image.

In Global Shutter, DATA_SEL is the input that makes the transition between the wavetables A and B. With DATA_SEL = 0, the sensor reads out according to the pattern of wavetable A, and with DATA_SEL = 1, the sensor reads out according to the pattern in wavetable B. The CIS2521 registers, including the wavetable registers, are loaded with default values at power-up (and also when RESETB = 0). These default values (and also the BAE-recommended ones to program in that are in the CIS2521 Programming Manual) assume that wavetable A is used for the Global Shutter Reset frame and wavetable B is used for the Global Shutter Data frame. Therefore, in order for the sensor to function in Global Shutter, the user must frequently be changing DATA_SEL from 0 to 1 and from 1 to 0.

The normal row readout pattern in a frame is: pre-scan rows, followed by dark rows, followed by the active imager rows. If there are pre-scan rows, making the DATA_SEL transition (0 = >1 or 1 = >0) and TX1 pulse during the pre-scan row readout is the safest: even if you don't make these actions during the CHARGE_TRANS low period, it doesn't matter since pre-scan rows (i.e. physically non-existent rows) are being read out.

In the most difficult case, when there are only active imager rows in the frame, problems can easily occur. Timing the DATA_SEL transition is done by monitoring the FVAL signal which drops briefly when a completed frame is read out at the digital outputs (DOUT/DOUT_LG pins). That is, FVAL dips briefly when the digital data for the last row in the frame appears on the DOUT/DOUT_LG pins. The analog data at the pixel level for this last row of the frame was read out 2 line times earlier (because pixel data readout is a three line time process: analog pixel readout, analog to digital conversion in the column amplifiers, and digital readout at the DOUT/DOUT_LG pins). The DATA_SEL transition should therefore have occurred 2 line times prior to the dip in the FVAL signal. To avoid complications of this sort, it is best to include some pre-scan lines in your frames when doing Global Shutter. Problems can be avoided with a simple formula:

1) Have a small number (at least 4) of pre-scan lines in each Global Shutter frame.
2) Make the DATA_SEL 0 = >1 and 1 = >0 transitions during the middle of the pre-scan period.
3) Make the TX1 pulse in the pre-scan period that marks the beginning of the Data frame (here assuming a standard readout order of pre-scan => dark => active imager).
4) The TX2 pulse can occur at any time, but must occur during a CHARGE_TRANS low period. (This rule can be ignored if the readout arrangement includes multiple Reset

frames prior to the Data frame, and the start of integration marked by TX2 occurs in one of the Reset frames other than the one immediately preceding the Data frame. This rule can also be avoided if integration times less than one line time are needed and the TX1 pulse takes place during pre-scan readout. In that case, the TX2 pulse will also take place during pre-scan readout and therefore have no effect on the imager regardless of the CHARGE_TRANS state.

5) For added (redundant) protection, the TX1 pulse can be limited to a CHARGE_TRANS low period, and the DATA_SEL transitions can be synchronous with a falling edge of CHARGE_TRANS low. The DATA_SEL 0=>1 transition and the TX1 rising edge would also be synchronous.

Note 3: VPTAT (Voltage Proportional to Absolute Temperature) should output a voltage over 2 Volts at room temperature which will vary linearly with temperature. The user should calibrate this output against an external temperature measuring device (e.g. a thermocouple on the back of the imager). A typical coefficient of voltage change to temperature change is 5 to 7 mV per degree Celsius.

Monochromatic Quantum Efficiency

Unless otherwise specified, this datasheet assumes the CIS2521 sensor is monochromatic (i.e. it has no color filter), and a typical monochromatic QE curve is shown in Figure 29. However, adding a color filter is an option with the CIS2521. The color filter spatial arrangement is shown in Figure 30 and the QE curves of the RGB color filters are shown in Figure 31.

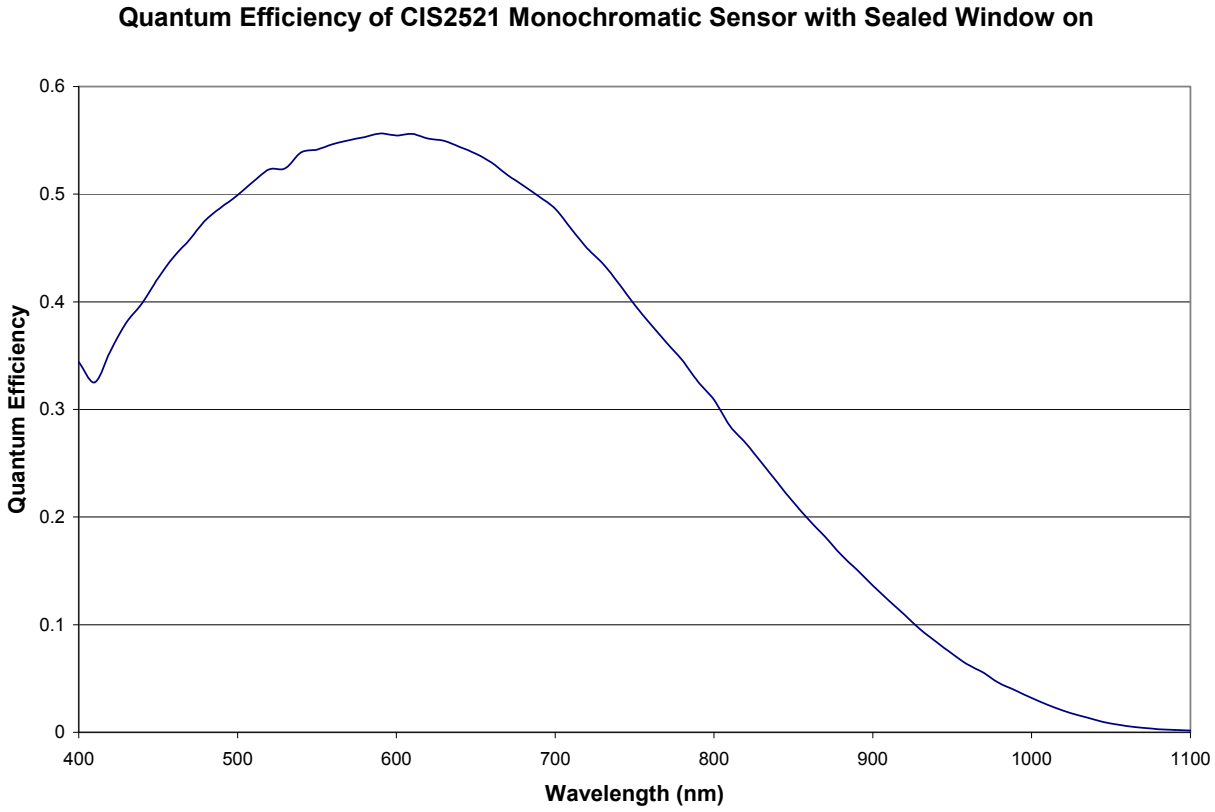
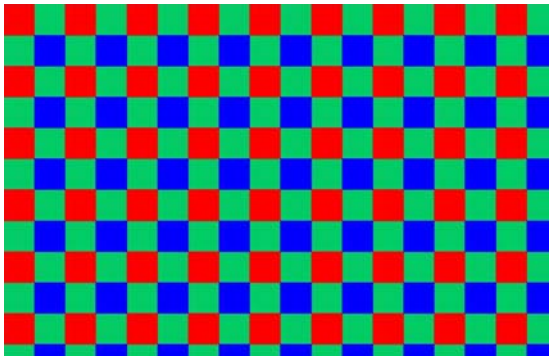


Figure 29. QE versus wavelength curve for monochromatic sensor

A table showing the monochromatic Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the Sealed window on.

WaveLength	Monochromatic	WaveLength	Monochromatic	WaveLength	Monochromatic
400 nm	0.34	640 nm	0.54	880 nm	0.17
410 nm	0.33	650 nm	0.54	890 nm	0.15
420 nm	0.35	660 nm	0.53	900 nm	0.14
430 nm	0.38	670 nm	0.52	910 nm	0.12
440 nm	0.40	680 nm	0.51	920 nm	0.11
450 nm	0.42	690 nm	0.50	930 nm	0.10
460 nm	0.44	700 nm	0.49	940 nm	0.08
470 nm	0.46	710 nm	0.47	950 nm	0.07
480 nm	0.47	720 nm	0.45	960 nm	0.06
490 nm	0.49	730 nm	0.44	970 nm	0.06
500 nm	0.50	740 nm	0.42	980 nm	0.05
510 nm	0.51	750 nm	0.40	990 nm	0.04
520 nm	0.52	760 nm	0.38	1000 nm	0.03
530 nm	0.52	770 nm	0.36	1010 nm	0.03
540 nm	0.54	780 nm	0.35	1020 nm	0.02
550 nm	0.54	790 nm	0.33	1030 nm	0.02
560 nm	0.55	800 nm	0.31	1040 nm	0.01
570 nm	0.55	810 nm	0.28	1050 nm	0.01
580 nm	0.55	820 nm	0.27	1060 nm	0.01
590 nm	0.56	830 nm	0.25	1070 nm	0.00
600 nm	0.55	840 nm	0.23	1080 nm	0.00
610 nm	0.56	850 nm	0.21	1090 nm	0.00
620 nm	0.55	860 nm	0.20	1100 nm	0.00
630 nm	0.55	870 nm	0.18		

Color Filter Array (CFA) Option



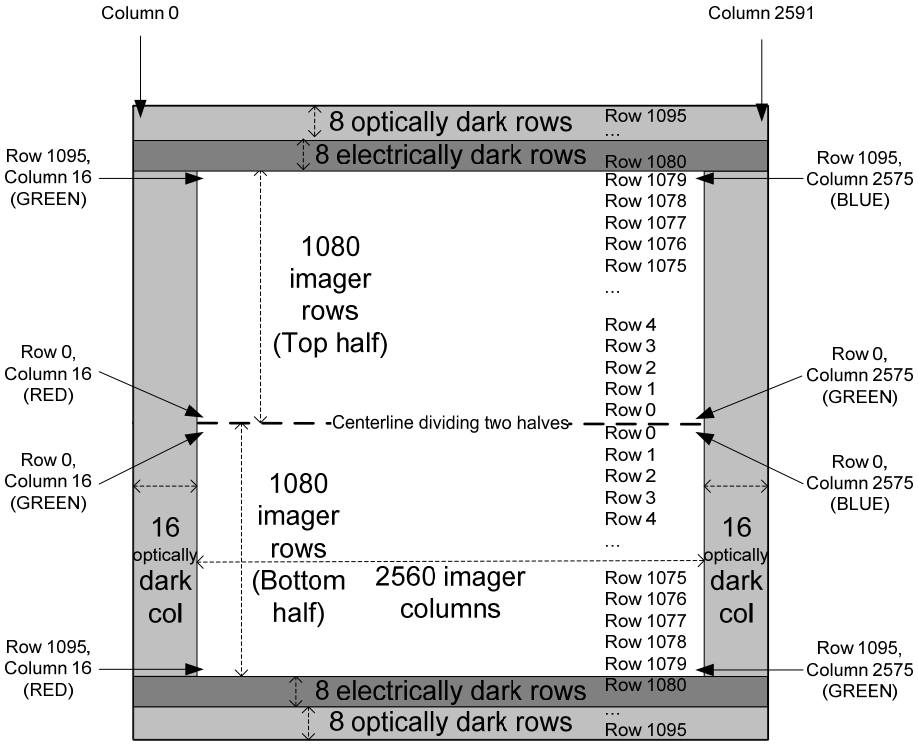


Figure 30. Color Filter Array

The Bayer pattern RGB Color Filter Array (CFA) covers the 2560 (H) x 2160 (V) imaging pixels and extends 2 pixels deep into the dark pixels region on all 4 sides.

For the top half of the sensor, even numbered rows are Red/Green, with even columns Red and odd columns Green. Odd numbered rows are Green/Blue, with even columns Green and odd columns Blue.
For the bottom half of the sensor, even numbered rows are Green/Blue, with even columns Green and odd columns Blue. Odd numbered rows are Red/Green, with even columns Red and odd columns Green.

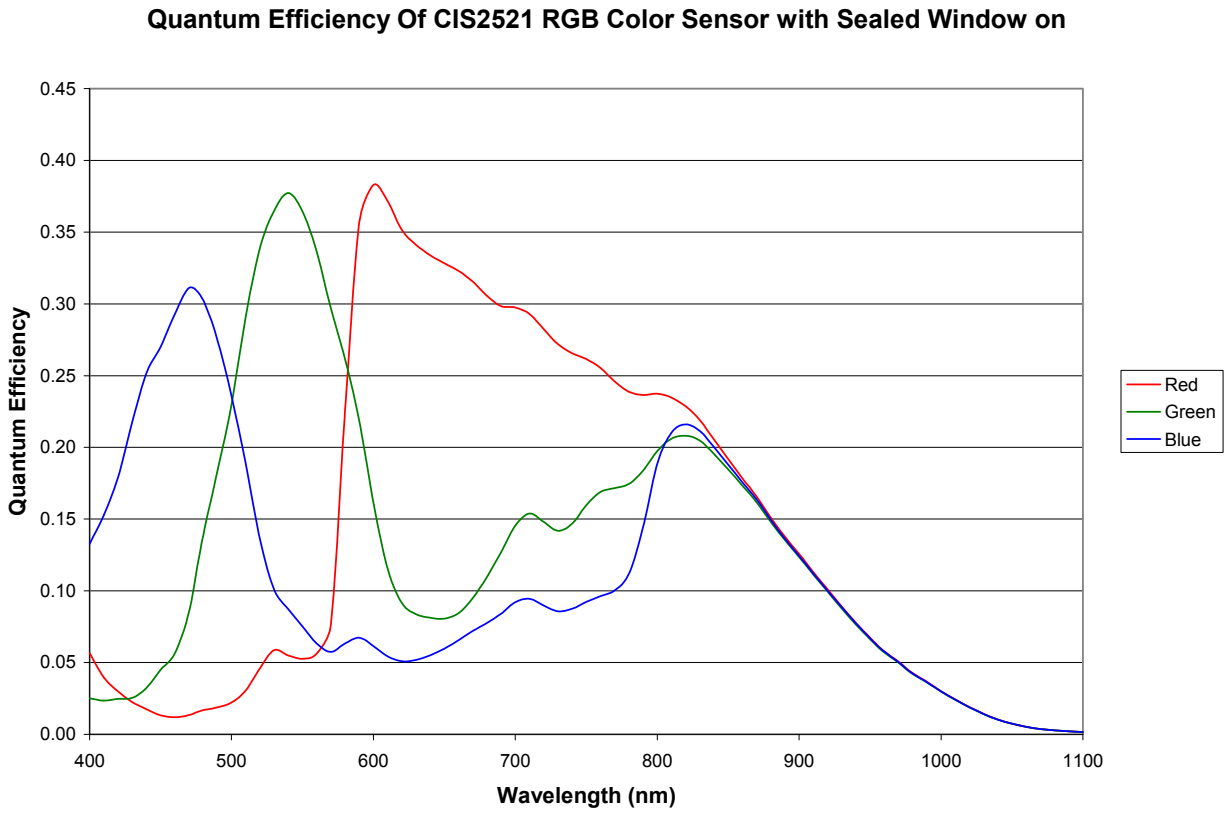


Figure 31. CFA QE Curves

A table showing the RGB color Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the Sealed window on.

WaveLength	Red	Green	Blue	WaveLength	Red	Green	Blue
400 nm	0.06	0.03	0.13	760 nm	0.26	0.17	0.10
410 nm	0.04	0.02	0.15	770 nm	0.25	0.17	0.10
420 nm	0.03	0.02	0.18	780 nm	0.24	0.17	0.11
430 nm	0.02	0.03	0.22	790 nm	0.24	0.18	0.14
440 nm	0.02	0.03	0.25	800 nm	0.24	0.20	0.19
450 nm	0.01	0.05	0.27	810 nm	0.23	0.21	0.21
460 nm	0.01	0.06	0.29	820 nm	0.23	0.21	0.22
470 nm	0.01	0.09	0.31	830 nm	0.22	0.20	0.21
480 nm	0.02	0.13	0.30	840 nm	0.21	0.20	0.20
490 nm	0.02	0.18	0.28	850 nm	0.19	0.18	0.19
500 nm	0.02	0.23	0.24	860 nm	0.18	0.17	0.18
510 nm	0.03	0.29	0.19	870 nm	0.17	0.16	0.16
520 nm	0.05	0.34	0.14	880 nm	0.15	0.15	0.15
530 nm	0.06	0.36	0.10	890 nm	0.14	0.14	0.14
540 nm	0.05	0.38	0.09	900 nm	0.13	0.12	0.12
550 nm	0.05	0.36	0.08	910 nm	0.11	0.11	0.11
560 nm	0.06	0.34	0.06	920 nm	0.10	0.10	0.10
570 nm	0.08	0.30	0.06	930 nm	0.09	0.09	0.09
580 nm	0.23	0.26	0.06	940 nm	0.08	0.08	0.08
590 nm	0.36	0.22	0.07	950 nm	0.07	0.07	0.07
600 nm	0.38	0.16	0.06	960 nm	0.06	0.06	0.06
610 nm	0.37	0.12	0.05	970 nm	0.05	0.05	0.05
620 nm	0.35	0.09	0.05	980 nm	0.04	0.04	0.04
630 nm	0.34	0.08	0.05	990 nm	0.04	0.04	0.04
640 nm	0.33	0.08	0.06	1000 nm	0.03	0.03	0.03
650 nm	0.33	0.08	0.06	1010 nm	0.02	0.02	0.02
660 nm	0.32	0.08	0.07	1020 nm	0.02	0.02	0.02
670 nm	0.32	0.09	0.07	1030 nm	0.01	0.01	0.01
680 nm	0.31	0.11	0.08	1040 nm	0.01	0.01	0.01
690 nm	0.30	0.13	0.08	1050 nm	0.01	0.01	0.01
700 nm	0.30	0.15	0.09	1060 nm	0.01	0.01	0.01
710 nm	0.29	0.15	0.09	1070 nm	0.00	0.00	0.00
720 nm	0.28	0.15	0.09	1080 nm	0.00	0.00	0.00
730 nm	0.27	0.14	0.09	1090 nm	0.00	0.00	0.00
740 nm	0.27	0.15	0.09	1100 nm	0.00	0.00	0.00
750 nm	0.26	0.16	0.09				

Cosmetic Specifications

Defect classification	Criteria	Maximum Count	Comments
Hot Pixels in Dark Frame	± 6 sigma from the mean	5000	Low gain only
Cold/Warm Pixels in Light Frame – Minor Defects	> 15% from the mean	5000	Low gain only
Cold/Warm Pixels in Light Frame – Major Defects	> 50% from the mean	25	Low gain only
Small Cluster in Light Frame – Qty Allowed	± 6 sigma from the mean 2 < Size <= 20pix	50	Low gain only
Large Cluster in Light Frame– Qty Allowed	± 6 sigma from the mean Size > 20pix	0	Low gain only
Column -- Qty Allowed	± 10% gain variation from the mean	0	Low gain only, Light frame – dark frame
Row -- Qty Allowed	Row 0: +15/-10% gain variation from the mean Row 1-999: ± 10% gain variation from the mean	0	Low gain only, Light frame – dark frame

Test conditions

Blemish tests are performed in Rolling Shutter mode; light frame captured at 50% of saturation.

Blemish specification applies to ROI: Center 2496 (H) x 2000 (V)

Storage Conditions

Parameter	Minimum	Maximum	Units
Temperature	-40	+85	ºC

Handling Precautions

To avoid damaging the device during handling, special care must be used with strict ESD controls. Use only ESD protected tools and ESD protected workstations. Operators must be equipped with approved ESD safe garments and use approved grounding equipment.

Soldering Instructions

Do not exceed peak temperature of 225C for more than 60 seconds. Follow temperature ramp guidelines in JEDEC/IPC standard J-STD-020, current revision, for the IR/Convection oven reflow profile. Alternative automated solder reflow methods have not been qualified or tested.

Window Cleaning Instructions

Only the window surface above the active area needs to be cleaned. Do not pour solvent or any liquid directly on to the window surface. Use a clean, lint-free swab. Dip swab in methanol or isopropyl alcohol and carefully wipe the surface of the window. Clean, dry air can also be used to blow particle contamination off the window.

Cleaning the sensor active area surface itself is generally not possible since the CIS2521 is almost always shipped with an epoxy-sealed window that covers the sensor active area. If it is possible to directly access the sensor active area, cleaning it is not recommended.

Sensor Package Cleaning Instructions

Use a clean, lint-free swab, dipping the swab in methanol or isopropyl alcohol and carefully wiping the sensor package. Acetone can also be used to clean the sensor package, but only if it can be kept away from the window seal epoxy. Clean, dry air can also be used to blow particle contamination off the window.

Revision History

Date	Revision	Description
June 2011	NR	Initial Release
July 2011	A	Incorporated Recommended Settings
March 2012	B	Deleted references to DOUT pins multiplexing, clarified DVDD_3V3 power on, added sealed window die stack up figure
August 2012	C	Added soldering and cleaning instructions. Added figure with row numbering. Extended pin descriptions and explanatory notes. Included Standard package drawing and updated Scientific package drawings. Changed sensor name from CIS2051 to CIS2521.
December 2012	D	Added die placement, tilt and rotation specs. Clarified standard package thermal pad grounding. Changed sensor nomenclature to have 4 digit suffix. Added revision disclaimer.
February 2013	E	Changed Standard Package drawings, fixed typos, clarified TX1 and TX2 current requirements for Global Shutter pulses. Added Standard package photo to front page. Added HSTL class number.

Disclaimer

BAE Systems reserves the right to make any changes to this product during an existing contract period providing it does not materially affect the form, fit or function of a Customer's next assembly product with BAE Systems' previously released design.

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